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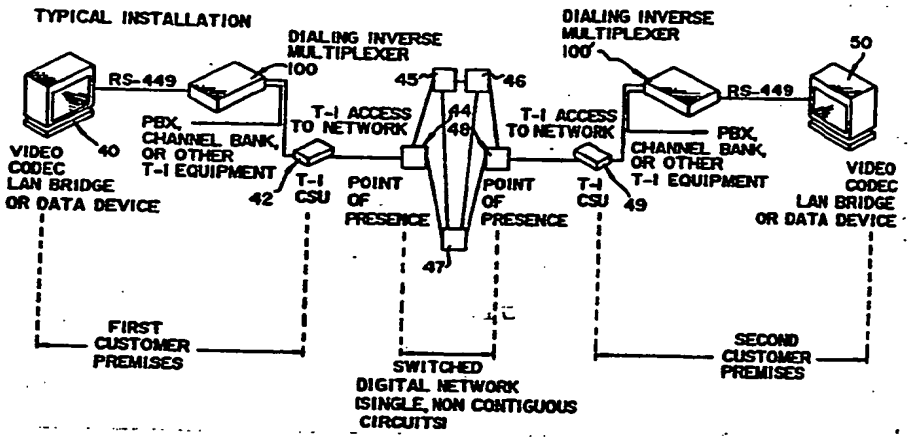

(57) Abstract

The present invention relates to the field of high speed data transfer for digital communications using communications networks having relatively narrow bandwidth time division multiplexed channels. The invention also relates to wideband communications using a plurality of time division multiplex channels having bandwidths which are individually insufficiently large to individually support the wideband communications. The apparatus for data communication includes a first interface arrangement for interfacing with a data communications network; a second interface arrangement for interfacing with a data source; and a data multiplexing arrangement for multiplexing data from the data source into a selected number of channels.

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APPARATUS FOR HIGH SPEED DATA TRANSFER

TECHNICAL FIELD

The present invention relates to the field of data communications. In particular, the present invention relates to the field of high speed data transfer for digital communications using communications networks having relatively narrow bandwidth time division multiplexed channels. The invention also relates to wideband communications using a plurality of time division multiplex channels having bandwidths which are individually insufficiently large to individually support the wideband communications.

BACKGROUND OF THE INVENTION

Digital communications can be carried on commercially available T-1 communication lines. Such communication lines are

described in tariff #270 filed by AT&T in 1982, which covers High Capacity Terrestrial Digital Service (HCTDS). According to this tariff, a T-1 communication line has a data transmission capability of 1.544 Mbps. A T-1 frame consists of 24 8-bit DS0 channels. The T-1 transmission rate utilizing DS-1 signalling can transmit 8000 frames per second, at 193 bits per frame, which yields a transmission rate of 1.544 Mbps. In a T-1 communication line link, DS-1 signalling is used. According to this type of signalling, the 24 channels, each of which comprise separate data streams, are transmitted as a single frame. Each channel contains 8 bits, for a total of 192 bits per frame. One additional bit is used in each frame for synchronization purposes, and accordingly a frame is actually composed of 193 bits. According to this standard, the rate of 8000 frames per second can be transmitted.

In many telephone systems, "robbed bit" signalling is used, which further reduces the usable capacity of each DS0 channel from 8 bits per frame to 7 bits per frame, reducing the capacity of a full frame from 192 bits to 168 bits, and thereby yielding a useful transmission rate of 1.344 Mbps. A DS0 can accommodate 64 kbps of bandwidth (8 bits x 8000 frames/sec). However, when "robbed bit" signalling is used to indicate on-hook and off-hook states, only 56 kbps of bandwidth is guaranteed to be switched for any DS0.

For higher speed transfer than that available by a single DS0 channel, it is known to employ a plurality of DS0 channels which are located together physically along the same telecommunications route. Such high data rate communications are needed by, for

example, video teleconferencing applications. For such data communications, however, it has been necessary to co-route all of the plurality of DS0 channels to guarantee simultaneous arrival without differences in propagation delay along diverse routes.

A typical interface provided for a T-1 multiplexer to an end user is the V.35 interface. For video teleconferencing, a video CODEC is used for converting an analog input signal into output binary bits. At the receiving end, a decoder converts the binary bits back to analog signals.

In practice, in known devices for sending large amounts of data, a plurality of contiguous DS0 channels must be used. In conventional long distance networks, each telephone circuit carrying the video telecommunications signal would travel by a different path. For example, a telephone communication between New York and California might travel via Atlanta or Chicago, and a large number of other switching paths are also possible. This gives rise to a synchronization problem when using a plurality of telephone channels to transfer large bandwidth data on a plurality of lower bandwidth lines. That is, since the transmitted data may be transmitted via different paths, different transmission times are involved, making it difficult to reassemble in real-time the arriving data into the original large bandwidth signal. This causes substantial delays to arise in setting up video conference calls, due to the necessity of waiting until the requisite number of contiguous T-1 communication lines have been obtained by the telephone company, as explained further below.

In the prior art, for high speed data transmission requiring use of more than one DS0 channel, a plurality of channels must be obtained by the telephone company which occupy consecutive multiplex timeslots. This solution, which is both relatively difficult to implement by the telecommunications company and relatively expensive to purchase, is well-known. In this type of service, a user communicates by telephone with the telecommunications company in advance, to obtain the video conferencing telecommunications service. After a wait of at least several minutes, and occasionally of one-half hour, the requisite number of physically contiguous lines are made available by the telecommunications company for use. This solution is relatively inefficient for the telecommunications company since it is relatively difficult to free up a plurality of consecutive timeslots. It requires an extensive search by the telecommunications company to obtain the requisite number of lines and to keep them clear for a predetermined or unknown length of time. Accordingly, even for a video teleconference of relatively short duration, for example several minutes, a minimum fee for one-half hour of telecommunications company service is often required at present. Additionally, because these lines are dedicated and can only carry the transmissions of the users involved in the video teleconference, the line charges themselves are relatively high.

On present telecommunications lines, a telephone call originating at a first location may be routed by any one of a relatively large number of different telecommunications paths.

Once a call has been routed to a receiving facility, the routing is not changed. This makes possible error-free transmission of data once the telecommunications path has been established. However, the specific path obtained is unpredictable, and the length of the communications delay is determined by the path length as well as by other factors such as whether a satellite link has been included in the path. This presents a problem in that, as discussed above, when sending large amounts of data over a plurality of telecommunications lines such as would be necessary in video teleconferencing, it is not possible with previous existing equipment to reconstruct in real time the original signal, since the individual telecommunications paths may be different.

It is additionally a problem in the prior art to use only a fraction of the total number of available channels commonly used with a T-1 communication link, instead of occupying all available channels, for providing telecommunications requiring bandwidths which are less than the entire bandwidth of the total number of available channels, yet greater than that available on a single one of the channels, while retaining the ability to use the remaining unused channels for other purposes such as voice telecommunications or the like.

Echo cancelling, which is used for voice telecommunications, must be shut off when sending digital data over a telecommunications line equipped to carry both voice and data. If, in a given telecommunications link, echo cancelling has not been turned off, data may be corrupted and lost. When using a plurality of T-1

channels for high speed data communications which must travel on a plurality of T-1 lines, and which do not travel along physically identical communication paths, it is a problem to identify which of the communication paths still has echo cancelling in effect. This is necessary so that another communications link can be established which does not have echo cancelling in effect, or to notify the telecommunications carrier of improper equipment operation along the specified communications route so that manual correction techniques can be applied, thereby enabling echo cancelling to be turned off along that telecommunications path for transmission of digital data.

Another problem in the prior art is to provide adjustable bandwidth data transmission over existing data communication lines. In particular, the prior art devices cannot provide a bandwidth over an arbitrarily large or small number of channels, up to the limit of the number of channels which can be handled by the communications device being used. It is in particular not known in the prior art to provide a bandwidth capacity based upon simultaneous use of only a portion of 24 available channels, nor is it known to simultaneously employ a number of these available channels for one purpose (such as digital video image data transmission) while employing remaining ones of the available channels simultaneously for other purposes (such as digital voice data transmission for a number of telephone calls), in which each channel carries data at a rate of at least 56 kbps.

It is a further problem in the art to simultaneously dial up a large number of channels for data transmission, due to the cumulative time delay involved in sequentially dialing up each of a plurality of telephone numbers. For example, an average dial-up time may be 15 seconds, including the necessary time for going "off-hook" (i.e. establishing a connection with the data carrier including receiving a "wink" signal), dialing the desired number, and establishing the connection with the receiving equipment at the remote location. For data transmission across a bandwidth of 24 channels at 56 kbps on each channel using sequential dial-up, the necessary waiting time for establishing communications on all 24 channels would take approximately 6 minutes. Therefore, known devices for dialing up a plurality of telephone numbers have the drawback of the above-mentioned relatively substantial delay in establishing all channels, and this constitutes an undesirable loss of time which could otherwise be used for data transmission.

Further, the known prior art devices do not provide the capability of automatically conducting a standard error rate test on each of a plurality of data communication lines, and taking out of service any lines which fail the standard error rate test. In particular, the known devices do not have a capability of simultaneously conducting a standard error rate test on a plurality of channels (e.g., 24 channels, each channel individually having a 56 kbps capacity).

Additionally, conventional data communication devices capable of transmitting data at relatively high rates cannot be operated

remotely. In particular, the conventional data communication devices do not enable remote access to all functions available at the front keyboard via a modem connection.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a device capable of selectable bandwidth, high speed data communications which can use a selectable number of data transmission channels.

It is a further object of the present invention to provide a device capable of selectable bandwidth, high speed data communications, which can use a selectable number of the 24 available data transmission channels of a T-1 frame.

It is a further object of the present invention to provide a device capable of selectable bandwidth, high speed data communications, which can use a selectable number of the 24 available data transmission channels of a T-1 frame, and in which the data carried by each channel need not travel along physically contiguous communication lines throughout the transmission path.

It is another object of the present invention to provide a high speed data communications apparatus for using a selectable number of data communication lines for sending data at high speed, and which is capable of employing different communication paths for each of the data communication lines, the apparatus also being capable of receiving data on each of the plurality of communication lines and reassembling the received data in a correct order to

obtain the original large bandwidth signal, regardless of the differences in delay times among the separate channels used, the different delay times being due to the different communications paths followed by each channel.

Another object of the present invention is to provide a high speed data communications apparatus for using a selectable number of data communication lines for sending data at high speed, and which is capable of dialing-up each required separate telecommunication line as a separate channel, in order to provide a selected bandwidth for data transmission.

A further object of the present invention is to provide a method for determining a correct sequence of received data frames received from a plurality of different telecommunications lines, for reassembling received data into a form corresponding to that sent at the transmitting location.

A still further object of the present invention is to provide data communications at a rate higher than 56 Mbps on a T-1 telecommunications line which is nominally rated at 56 Mbps.

It is another object of the present invention to provide user data rates in 8 kbps increments by dialing 56 kbps circuits and only using the bandwidth in the last connected channel which is needed. E.g., for a user rate of 384 kbps, 7 channels are dialed, giving a capacity of 392 kbps, but only 48 kbps of the 7th channel is used to deliver 384k to the user.

It is a still further object of the present invention to provide an apparatus capable of using a selectable number of T-1

lines out of a total number of available T-1 lines for high speed data communication, while permitting use of the remaining T-1 lines for other forms of communication.

It is a still further object of the present invention to provide an apparatus for high speed data communications using a plurality of separate channels on a T-1 line, and which is capable of automatically dialing up only the needed number of channels to establish the necessary bandwidth to be used for a particular data transmission.

It is a further object of the present invention to provide an apparatus for determining a relative network delay for each channel of a selected plurality of channels dialed-up and transmitted to a distant location, in order to determine a correct sequence of the received data for each of the plurality of selected channels.

It is another object of the present invention to provide an apparatus and method for determining whether a given T-1 line is improperly being subjected to echo cancelling, so that corrective action can be taken.

It is another object of the present invention to provide an apparatus and method for providing an adjustable operational bandwidth capacity over an arbitrarily large or small number of channels, up to the limit of the total number of channels which are connected to the communications device, which is a dialing inverse multiplexer, according to the invention.

More specifically, it is another object of the invention to provide an adjustable bandwidth dial-up capacity of up to 24

channels, each channel carrying data at a rate of at least 56 kbps.

It is another object of the present invention to provide an apparatus and method for automatically conducting a standard error rate test on each of a plurality of data communication lines. More specifically, it is an object to provide an apparatus and method for automatically conducting a standard error rate test on each of a plurality of data communication lines and taking out of service any lines which fail the standard error rate test.

In particular, it is another further object of the invention to provide an apparatus and method of simultaneously conducting a standard error rate test on a plurality of channels (e.g., 24 channels, each channel individually having a 56 kbps capacity), and automatically conducting a standard error rate test on each of these channels.

It is another object of the present invention to provide an apparatus and method for transmitting data at relatively high rates which can be operated remotely.

It is a further object of the present invention to provide remote access to all functions which are available at a front keyboard of a remote dialing inverse multiplexer communications device, via an RS-232 modem connection.

The invention will be described in greater detail below with reference to an embodiment which is illustrated in the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 schematically illustrates interconnection of components to a digital network, for providing digital communications between two different sites, according to the present invention.

Fig. 2 is a schematic diagram of the connection of a dialing inverse multiplexer according to the present invention with data input and output devices, and with a drop-and-insert PBX.

Figs. 3A-3D show framing organization of data according to T-1 standards, as used in the dialing inverse multiplexer according to the present invention.

Fig. 4 is a simplified flowchart depicting operation of the dialing inverse multiplexer according to the present invention.

Fig. 5 is a schematic diagram of circuit elements used in the dialing inverse multiplexer according to the present invention.

Fig. 6 schematically illustrates port connections to the ADD and DROP matrices of Fig. 5, depicting examples of channel usage according to the present invention.

Fig. 7 is a schematic illustration of a 4-port clock distributor used in the dialing inverse multiplexer of Fig. 5, according to the present invention.

Fig. 8 schematically illustrates the PRBS generator of Fig. 5, according to the present invention.

Fig. 9 schematically illustrates the PRBS receivers of Fig. 5, according to the present invention.

Fig. 10 schematically illustrates operation of the 6-pattern generator of Fig. 5, according to the present invention.

Fig. 11 schematically illustrates operation of the frequency synthesizer depicted in Fig. 5, according to the present invention.

Fig. 12 schematically illustrates operation of the signalling capture element of Fig. 5, according to the present invention.

Fig. 13 schematically illustrates operation of the data capture element of Fig. 5, according to the present invention.

Fig. 14 schematically illustrates the synchronizer of Fig. 5, according to the present invention.

Fig. 15 schematically illustrates operation of the 4-port elastic store/DROP of Fig. 5, according to the present invention.

Fig. 16 schematically illustrates operation of the 4-port elastic store/ADD of Fig. 5, according to the present invention.

Fig. 17 schematically illustrates the ADD multiplexer of Fig. 5, according to the present invention.

Fig. 18 schematically illustrates operation of the loopback controller of Fig. 5, according to the present invention.

Fig. 19 is a simplified flowchart depicting operation of another embodiment of the dialing inverse multiplexer according to the present invention.

Fig. 20 schematically illustrates a T-1 receive section, according to the present invention.

Fig. 21 schematically illustrates interconnection of components to a digital network, for providing digital communications between two different sites, and operating according to V.35 standards, according to the present invention.

Fig. 22 shows a table for a synchronizing pattern, according to the present invention.

Fig. 23 illustrates a received data pattern caused by differing delays on three transmitted channels, according to the present invention.

Fig. 24 illustrates generically how received data appears in memory, in the example of Fig. 23.

Fig. 25 shows a data arrangement in memory resulting from the examples of Figs. 23 and 24.

Fig. 26 illustrates a procedure for determining offsets of addresses for each channel in the buffer memory, according to the present invention.

Fig. 27 schematically illustrates operation of a circular buffer usable in the present invention.

Fig. 28 is a schematic diagram of circuit elements used in another embodiment of the dialing inverse multiplexer according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A typical installation of a single dialing inverse multiplexer according to the present invention is depicted in Fig. 1, indicating a customer installation connected to a point of presence 44 on a switched 56 kbps/sec digital network. A T-1 channel service unit (CSU) 42 is connected to the point of presence 44 and is connected for communication with a dialing inverse multiplexer 100 according to the present invention. The dialing inverse

multiplexer 100 can be connected to a variety of different devices, including a video CODEC 40, and can simultaneously be connected to a PBX, a channel bank, or other T-1 equipment. The video CODEC 40 can be replaced with a LAN bridge or other data device in the example of Fig. 1. The T-1 CSU 42 is a standard device. The CODEC 40 is also a standard device.

The network connections shown in Fig. 1 are schematic, and are representative of various connections which might occur among points 44, 45, 46, 47, and 48 when using a plurality of single, non-contiguous circuits. Points 44-48 indicate network switch sites; for example, 44 = Wash D.C., 45 = Chicago, 46 = Denver, 47 = Atlanta and 48 = Los Angeles.

The point of presence 48 provides T-1 access to the network for a T-1 CSU 49 which is located at a second customer premises distant from the first customer premises. The network connections shown could include a variety of additional network paths, any of which may include a path including a satellite link. In the example arrangement of Fig. 1, a plurality of DS-0 channels are used to connect the first and second customer premises in order to provide a very high bandwidth transmission. Each of the DS-0 channels may be carried along a different network path, resulting in different times of reception at the point of presence 48.

At the second customer premises, the TS-1 CSU 49 is connected to another dialing inverse multiplexer 100' which in turn can be connected to a video CODEC 50. The video CODEC 50 can be replaced by a LAN bridge or other data device, and the dialing inverse

multiplexer 100' can simultaneously be connected to a PBX, a channel bank, or other T-1 equipment. Furthermore, the dialing inverse multiplexers 100 and 100' can also be connected to other dialing inverse multiplexers of the same kind.

In Fig. 2, a "west" switch 20 is connected to an "east" PBX 22 via the dialing inverse multiplexer 100 (indicated in dotted outline). The dialing inverse multiplexer includes a D/I "west" branch element 30. The branch element 30 picks up a signal from line 28 and supplies the signal to an output device 26. The output device 26 can be a video display device, data router and so on. A D/I "east" branch element 32 selectively transmits a signal either from the PBX 22 or from the output device 26.

Figs. 3A-3D illustrate for reference purposes the T-1 digital transmission standards. Fig. 3a shows a single channel containing 8 bits. Fig. 3b illustrates a frame containing 24 separate channels plus one frame bit used for synchronization purposes. Therefore, a frame is actually composed of 193 bits.

Fig. 3c illustrates a group of 24 frames, which together form a superframe. Each frame can be transmitted in 125 microseconds so that a superframe is transmitted in 3 milliseconds as shown in Fig. 3d.

Fig. 4 is a flowchart depicting use of the dialing inverse multiplexers 100 and 100' for data communication, according to the present invention. To initiate data communication as indicated at block 500, the "DIAL" function is selected at block 501 from the unit keyboard. At block 502, the local dialing inverse multiplexer

100 goes "off-hook" and waits for a "wink" (i.e. dial tone) to occur, and as indicated at block 503, if the wink is received then the first telephone number of the remote dialing inverse multiplexer 100' is dialed as indicated at block 504. If the wink is not received, then the dialing inverse multiplexer 100 continues to wait until either a wink is received, or a preset time (e.g., 4 seconds) has expired.

As indicated at block 505, the remote dialing inverse multiplexer 100' answers and connection is established, after which a 2100 Hz tone is sent from the dialing inverse multiplexer 100 to disable the echo cancelers. The dialing inverse multiplexer 100 then sends a PRBS (psuedo-random bit sequence), which used in a standard error rate test known in the communications industry, to the remote dialing inverse multiplexer 100', as indicated at block 507. The error rate on the line is then tested at block 508, and if below a predetermined threshold (e.g., 1 bit error per thousand bits), then as indicated at block 510, the dialing inverse multiplexer 100 requests configuration data for the remote dialing inverse multiplexer 100'. If the error rate is too high, i.e. is greater than the predetermined threshold value, then the dialing inverse multiplexer 100 goes on hook to disconnect the line, and re-dials as indicated at block 509. In that case, the sequence of events is repeated beginning at block 502.

After configuration data is requested at block 510, the dialing inverse multiplexer 100 selects a transmission bandwidth based upon the configuration of the remote dialing inverse

multiplexer 100'. For example, if the local dialing inverse multiplexer 100 has a 16 channel capacity and the remote dialing inverse multiplexer 100' has only an 8 channel capacity, then the dialing inverse multiplexer 100 would select a bandwidth appropriate for the 8 channel capacity of the remote dialing inverse multiplexer 100', i.e. 8 channels. Then, as indicated at block 512, the local dialing inverse multiplexer 100 goes off-hook on the additional number of channels N necessary for the selected bandwidth.

In dialing the additional number of channels N necessary for the selected bandwidth, it is preferred that all of the N channels be dialed nearly simultaneously, to save on call set-up time. In this regard, it would be possible to use N standard dialing devices all controlled to dial each of the telephone numbers received in the configuration data supplied from the remote dialing inverse multiplexer 100' (or which was pre-stored in the local dialing inverse multiplexer 100). Special circuit arrangements can also be designed for this purpose.

For each of the N additional channels which go "off-hook" at block 512, it is determined at block 513 whether a wink start signal is received. If not, waiting occurs as indicated at block 514. If the winks are received, then each remaining one of the N additional numbers is dialed up as indicated at block 525. The remote dialing inverse multiplexer 100' then answers on each line as indicated at block 515. In practice, one or more channels of the remote dialing inverse multiplexer 100' may be busy or

otherwise out of service, and in this event the local dialing inverse multiplexer 100 is preferably programmed to re-dial two more times to attempt to make a connection. The number of re-tries is arbitrarily selected, however, and any number of re-tries (or no re-tries) can be chosen.

As indicated at block 516, upon completion of connection of the channels, a 2100 Hz tone is sent from the local dialing inverse multiplexer 100 to cause echo cancelers to be disabled on each of the channels. The local dialing inverse multiplexer 100 then transmits the PRBS on each of the N channels (or the successfully connected lines if fewer than N channels are successfully connected), as indicated at block 517. If the error rate is less than a threshold, as indicated at block 518, then the local dialing inverse multiplexer 100 sends a pattern to the remote dialing inverse multiplexer 100′ to determine channel alignment as indicated at block 520. Otherwise, the channel(s) having the unacceptable error rate is (are) re-dialed, as indicated at block 519.

After sending the channel alignment pattern at block 520, channel alignment is determined, as indicated at block 521. Then, a synchronizing pattern is sent from the local dialing inverse multiplexer 100 to the remote dialing inverse multiplexer 100′ as indicated at block 522, after which synchronization and channel delays are determined as indicated at block 523. The synchronization is necessary to determine the relative time delays which occur among the connected lines, so that, taking into account

the alignment data, the original data transmitted from the local dialing inverse multiplexer 100 to the remote dialing inverse multiplexer 100′ can be reconstructed at the remote dialing inverse multiplexer 100′.

After synchronization has been determined at step 523, data transmission begins, as indicated at block 524, on all N channels simultaneously.

Fig. 5 is a detailed schematic diagram of elements forming the dialing inverse multiplexer 100. The dialing inverse multiplexer 100 includes element sub-groupings 101 and 102.

The sub-grouping 101 of the dialing inverse multiplexer 100 functionally includes LED driver circuit 100, RS-366 interface circuit 112, LCD display circuit 114, and keypad drivers circuit 116, all of which are connected to a central processing unit (CPU) 300. The CPU 300 can be operated consistently with the foregoing according to a program which would be within the ambit of one ordinarily skilled in the programming art, and communicates with a memory 801. The memory 801 can contain various types of stored information, for example lists of telephone numbers, and so on.

A T-1 receive/transmit interface 106 receives signals at a network interface (NI) receive line and transmits output signals to a network interface (NI) transmit line, as seen in Fig. 5. Similarly, a T-1 interface 104 outputs T-1 transmission signals from a customer interface (CI) element 106 and outputs these signals on a customer interface (CI) transmit line. The T-1 interface 104 receives T-1 signals on a customer interface (CI)

receive line, and outputs these signals via a line 107 to a 16-port ADD ID matrix 140, an ADD data multiplexer 148, and a 6-pattern generator 230. A line 103 connects the interfaces 104 and 106 for receiving signals from the network interface receive line, and a clock generator 105 is connected to the line 103. The clock generator 105 supplies an output signal to a clock distributor 150, which is a 4-port clock distributor, and to a frequency synthesizer 310.

The clock distributor 150 receives an output signal from the frequency synthesizer 310, and supplies an output signal to an elastic store/DROP circuit 180 which has a 4-port structure. The output signal from the frequency synthesizer 310 is also supplied to an expansion connector 220.

A line 108 is connected to the line 103 for picking up a received signal from the T-1 interface 106, and this received signal is supplied by the line 108 to a 24-channel signalling capture element 240, a select channel data capture element 250, a serial-to-parallel converter 260, and a 16-port DROP ID matrix 142. The circuit portion 101 also includes a 4-port V.35 driver/receiver 120 having four input/output ports for data reception/transmission from/to the data device (e.g. CODEC). The driver/receiver 120 supplies an output signal to a loopback controller 190. The loopback controller 190 has an output signal which is supplied to an input of the driver/receiver 120.

In the circuit portion 102, a connector data port 210, which supports 16 data ports, supplies and receives signals to/from a 16-

port V.35 device (not shown) and a V.25 bis device (not shown).

When signals are received from the CI receive line 107 by the interface element 104, an output signal is supplied along the line 107 to the ADD I/O matrix 140 which in turn supplies 16 output signals, one for each port, a 20-bit PRBS generator 146, the ADD data multiplexer 148, a 4-port elastic store/ADD circuit 170, and to the expansion connector 220. The PRBS generator 146 supplies an output signal to the ADD data multiplexer 148. The ADD data multiplexer 148 additionally receives the output signal from the 6-pattern generator 230, the output of the 4-port elastic store/ADD circuit 170, and an input from the expansion connector 220. The ADD data multiplexer 148 then produces a multiplexed output to the interface element 106 for transmission of the signal on the NI transmit line. The 6-pattern generator supplies its output signal to the multiplexer 148 and to the expansion connector 220.

The DROP I/O matrix 142 supplies 16 output signals, one for each port, to the 4-port elastic store/DROP circuit 180, the expansion connector 220, and PRBS receivers 160. The receivers 160 are both a 9-bit PRBS receiver and a 20-bit PRBS receiver.

The serial-to-parallel convertor 260 supplies its output signal to the delay equalization buffer 270. The buffer 270 is a 340-millisecond delay equalization buffer which stores received data on all channels and allows the synchronizer access to all data captured within the previous 340 milliseconds. The buffer 270 supplies its output signal to a synchronizer 280 which in turn supplies its output signal to a parallel-to-serial convertor 290.

The parallel-to-serial convertor 290 supplies its output signal to the PRBS receivers 160, the elastic store/DROP circuit 180, and the expansion connector 220.

The clock distributor 150 supplies its output signal to the elastic store/ADD circuit 170 and to the elastic store/DROP circuit 180. The elastic store/DROP circuit 180 supplies its output signal to the loopback controller 190. The loopback controller 190 supplies one output signal to the elastic store/ADD circuit 170. The loopback controller 190 supplies another output signal to the V.25 bis insertion circuit 200. The V.25 bis insertion circuit 200 sends and receives signals to and from the connector data port 210.

With regard to how the dialing inverse multiplexer dials, it does this through the ADD data multiplexer 148. The mechanism is that DTMF tones are digitally represented by repeating patterns, and can be switched into the T-1 data stream through this ADD data multiplexer 148. Fig. 5 shows the six pattern generator 230, which allows 6 different patterns to be enabled and selected into the channels of the T-1 telecommunications line.

The procedure for simultaneously dialing on all channels is for one of the patterns to represent all of the digits there required, and software then enables these patterns into the channel in the T-1 at specific intervals that represents the particular digit that needs to be dialed. That is, every 100 milliseconds the pattern will increment from the tones representing digit 0 to digit 1, to digit 2, and all the way to 9, and will then repeat. Then those digits are considered valid for a short period of time, for

example about 50 milliseconds, then the software is used to decide which channels of the T-1 are to get which digit at a particular time, and software masks are set up so that idle time is enabled for the digits that are not needed. The digits that do need to go out on the channels are enabled at specific times and are not allowed to be transmitted at the other times.

Fig. 5 schematically shows the add ID matrix 140 and the drop ID matrix 142. The ID matrix concept is common to both the add side and the drop side, the add side being data transmitted to the T-1 telecommunications line and the drop side being data taken from the network T-1 telecommunications line.

In Fig. 6, an ID matrix is shown corresponding to either one of the matrices 140 and 142. The top row lists column headings for 16 ports, numbered 1 through 16 consecutively, while the left column represents channels 1 through 24 (only channels 1 through 5 are shown enabled), each channel having bits numbered 1 through 8. Examples of different bandwidths on different channels being supplied through ports 1 and 2 are depicted in Fig. 6. During actual operation, only non-overlapping ones (i.e., having non-overlapping channels) of the above-noted ports would be in use.

Fig. 6 shows the channels numbered 1 through 24 along the left side of the drawing, and is for the standard D4 framing. This framing scheme can apply for standard D4 framing or can be adapted for other framing schemes. Horizontally across the top of Fig. 6 are the numbers 1 through 16 representing the number of ports available on the dialing inverse multiplexer 100. The number of

ports selected is arbitrary, and could be extended to an arbitrarily large number indefinitely.

The ports in Fig. 6 are shown as being sixteen in number, the ports being numbered consecutively as port numbers 1 through 16. Shown in this figure, blocked off for port 1 are 7 out of 8 bits of channels 1 and 2. Each block bit represents 8 kilobits of data. The first seven bits of channel 1 represents 56 kilobits of data, and the first 7 bits of channel 2 represents another 56 kilobits of data. These arrangements are set up by the software in this matrix format (as described further below) so that, depending on the user's bandwidth needs, the user can establish a connection with n times 8 kilobits of data capacity to the network. For port 2 in Fig. 6, there are enough bits "enabled" on port 2 as shown, to support 128 kilobits of data. This would require dialing up three channels and using only part of the bandwidth of the third channel, as shown in Fig. 6, at port 2. In this example, only two of the seven 8-kilobit data slots in Channel 5 are required for the desired user bandwidth. The other five data slots in Channel 5 would be "padded" with ones just to maintain the well-known "ones density" requirement. The specific configuration shown in Fig. 6 is arbitrary, and depends on the selected bandwidth, port selected, and so on.

The remaining 14 ports in the example of Fig. 6 would, in this example, not be used for data transport. Some of the ports could be enabled in parallel on the drop side, that is, data coming from one distant source can be "dropped" to (received at) multiple ports

at the receiving dialing inverse multiplexer. If two different ports are to be used to receive the same information, then the block bits of the channels on the DROP ID matrix would be enabled for both ports. For example, if port 5 was required to receive the same data as port 1, then software would block in port 5 the first 7 bits in channel 1 and the first 7 bits in channel 2, and then port 5 would be receiving the same data as port 1. This represents a very flexible architecture for performing addition and dropping of 8 kilobit bandwidth to and from a network which might be formed by a plurality of dialing inverse multiplexers communicating with each other in a network formation.

Each of the ports in the example shown in Fig. 6 carries different data rates. The dialing inverse multiplexer 100 according to the present invention, using the ADD matrix 140 and the DROP matrix 142, enables selection of the number of channels to be used, the particular channels to be used, and even permits selection of the number of bits in a channel for fractional channel usage, all depending upon the required data rate. For example, in Fig. 6, port 1 carries data at a rate of 112 kbps on channels 1 and 2, whereas port 2 carries information at a rate of 128 kbps and uses channels 3, 4 and of 1/4 of channel 5. The ability to use fractional portions of individual channels is discussed further in the following.

Each port in Fig. 6 has control over the entire T-1 bandwidth. While 16 ports are shown, any number of ports could be designed in. For example, only four ports could be used, and alternatively, more

than sixteen ports could also be provided. The bandwidth can be shared with different ports on the DROP side, although not on the ADD side. That is, the bandwidth can be shared with different ports when using the DROP ID matrix 142 but not when using the ADD ID matrix 140.

Figure 7 is a schematic diagram depicting the 4-port clock distributor 150 of Fig. 5. This figure shows four ports implemented, in which each of the clock selectors represented by blocks 155, 156, 157, and 158, are multiplexers, one for each of Ports 1-4, and are identical. The clock selectors 155-158 respectively supply output signals labelled as Port 1 clock, Port 2 clock, Port 3 clock, and Port 4 clock.

The 4-port clock distributor 150 shown in Fig. 7 receives clock signals of 1344 kHz (56kHz time base) and of 2048 kHz (64kHz time base) by dividers 152 and 154, respectively, from the microprocessor (CPU) 300. The microprocessor 300 produces a control signal which is supplied to selection registers 151. The selection registers 151 include a Port 1 clock select register, a Port 2 clock select register, a Port 3 clock select register, and a Port 4 clock select register. The port clock select registers for Ports 1-4 of the selection registers 151 respectively supply their output signals to the clock selectors 155-158 and determine which of the sixteen frequencies is multiplexed to the port n clock lines.

The microprocessor (CPU) 300 is used to select which of the 16 inputs are to be selected to the clocks which will drive another

block called the elastic stores. This entire section is a way of selecting a specific clock rate for the user. The clock rates are in specific, predetermined increments, and such clock rates are selected to include all of the most frequently used data frequencies that most users are likely to use for their equipment.

The selection registers 151 discussed above, which include port clock select registers for Ports 1-4, are registers which the microprocessor (CPU) 300 will write to, and there are four registers at element 151, one for each of the clock selectors 155-158. For the clock selector 155 for Port 1, for example, there are 16 different clock sources, supplied by the dividers 152 and 154, that can be enabled onto the port 1 clock by selection by the clock selector 155. Each of these clock sources is at a different frequency, and these frequencies are synthesized by the dividers 152 and 154. The dividers 152 and 154 include a known type of circuitry that takes a signal from a master clock and divides this frequency to the various specified rates as shown being supplied to the clock selectors 155-158. Additionally, another input port can be provided to the clock selectors 155-158, not shown, which can be chosen to receive an external synthesized frequency supplied by a user, for example for a special purpose requiring a frequency not supplied by the dividers 152 and 154.

The essence of this 4-port clock distributor 150 is to provide a clock source to the user at the same rate that the data will be added and dropped from the dialing inverse multiplexer 100 to/from

the data device, such as a CODEC or a video teleconferencing bridge, or a data router for example.

With regard to the CPU 300 selecting what to put in each of the registers at block 151, the following applies. The user would determine what frequency to operate at. A typical frequency might be 448 kbps for a video teleconference, for example. With the four ports that are currently implemented, if a user on Port 1 wishes to dial a circuit at 448 kbps, the user would supply a command to any of several different available interfaces which could be provided for operating the dialing inverse multiplexer 100.

Take, for example, the provision of a front input panel having a key pad and an LCD display (not shown) on the front panel of the dialing inverse multiplexer 100. In this case, the user could select a rate of 448 kbps for Port 1. In this case, a software map (not shown) of a conventional type would be provided to be accessible to the CPU 300. This map is thus usable by the CPU 300, in a known manner, to place the actual bit representation of 448 (i.e., in this example, the value of the selected frequency in kilohertz) into a selection register which corresponds in Fig. 7 to the sixth input line down supplied from the dividers 152 and 154 into the clock selector 155. Once that is done, then the data interface then should have a clock rate of 448 kbps, that after a telecommunications circuit is established through the dialing protocol, would then deliver a data rate of 448 kbps of data through the T-1 telecommunications line to the second, remote site.

In summary, the dividers 152 and 154 supply output signals at various multiples of the input time base, as shown in Fig. 7, to clock selectors 155, 156, 157, and 158. The clock selectors 155-158 of Fig. 7 respectively supply port clock output signals for Ports 1-4, respectively. The clock selectors 155-158 respectively receive port clock select signals from selection registers 151. The CPU 300, as discussed above, supplies a control signal to the selection registers 151 to control the selection.

The PRBS generator 146 is shown in Fig. 8. A 20-stage (2e20)-1 PRBS generatqr (which is known in the art) is used in the example of Fig. 8. The PRBS generator 146 receives a clock enable signal, port 8 add valid, and outputs PRBS data.

The initials PRBS of the PRBS generator 146 of Fig. 8 stand for "pseudo random bits sequence". It represents a known way of generating bits which appear to be random and that are not in any particular sequence. The phrase "pseudo random" means that the sequence of bits produced is not purely mathematically random, but does repeat. In Fig. 8 this generator produces a pattern which repeats every 2 to the 20th minus 1 bits, which is a little over a million bits. It is referred to as a 20 stage PRBS generator, and it is known to implement this in a fairly straightforward way using circuit flip-flops and common gates in a circular shift register with feedback arrangement. This is a fairly standard implementation that is used in the industry to generate pseudo random data.

In Fig. 9, an arrangement 160 is shown having two PRBS receivers 160a and 160b. The reason that there are not two PRBS generators 146 in Fig. 88 is that a random pattern is used that repeats every 511 bits, and is implemented through software pattern generation and not shown here since Figs. 8 and 9 represent physical hardware elements. The 511 pattern repeats often enough that it can be a simple look-up table in software and inserted into the T-1 telecommunications line by one of the pattern generator selections that is described earlier with regard to the six pattern generator 230. The arrangement 160 is the receiver for each of psuedo random generators. The receivers 160a and 160b normally are loaded periodically when it is determined that a certain number of errors have occurred.

A standard implementation of the PRBS generators and receivers is for performing error testing through the telecommunications network. For example, in performing such testing, Site A will send pseudo random data through all the channels that are connected, using the entire bandwidth that the user may select for a particular dialing sequence and, since the predetermined PRBS pattern has been pre-selected as noted above and is therefore known to be sent from Site A, this predetermined pattern should be received at the distant end, Site B, having an identical implementation on the receiver. Two sets of data, i.e. the received data at Site B and the data generated by the local PRBS receiver at Site B, are then made to be in phase so that every bit coming in from the network can be compared to a known ("good") bit

from the local receiver, and if there any network impairments that will cause error in any bit, such impairments will show up immediately on the aforementioned comparison which takes place on a bit-by-bit basis. These errors are logged in counters 160c and 160d shown Fig. 9. The counters 160c and 160d are then read by software sufficiently fast enough so that they do not overflow. Software is provided for keeping a much larger count of errors to prevent overflowing, and therefore store up to many millions of bit errors that may be recorded.

In summary, the PRBS receiver 160 illustrated in Fig. 9 includes two parallel PRBS receivers (each corresponding to a different PRBS implementation described above, i.e. the "511" pattern (receiver 160a) or the "2 to the 20th minus 1" pattern (receiver 160b) receiving input data and producing error signals to the respective modulo 256 counters 160c and 160d. As seen in Fig. 9, the modulo 256 counters are connected to the CPU 300.

Fig. 10 schematically depicts the 6-pattern generator 230, which includes for each of the six patterns a holding register 230a and a circular shift register 230b. The holding register 230a is updated once each T-1 frame by the microprocessor 300. The shift register 230b shifts continuously and is loaded with the holding register contents at T-1 frame boundaries.

The 6-pattern generator 230 was described above with regard to the insertion of DTMF tones used for the "dialing", and is a shift register that is updated by software to generate the DTMF tones. The DTMF pattern represents an 8 bit sample of a tone, i.e. a

frequency. The frequency is repeating a certain number of samples which are required to generate the tone, and it also is a repeating sequence as well. Typically anywhere from approximately 30 to 120 8-bit bytes are required for any given DTMF tone to generate the digits zero through 9. The pattern generator 230 is also used for sending out echo canceler disable tones, which is another tone at 2100 hertz. It is also usable for a method in which two dialing inverse multiplexers 100 are used to communicate with each other. That is, a specific pattern would be loaded and repeated and written by software to these registers, to enable them to read channels that are required to communicate with a remote unit. Since there are six of these patterns which can be generated by the pattern generator 230, it is possible to dedicate patterns for multiple specific features. For example, Pattern 1 can be dedicated to the DTMF tones, that is, all that the software needs to do is direct the CPU 300 to load this register with the tones and then at the proper time, allow the ADD data multiplexer 148 to select the tones onto the channel that is required to do the dialing. Then for another port that is in a different phase of call setup, Pattern 2 can be the echo canceler tone which can be enabled to the channels currently dialed for Port 2. Pattern 3 could be a message that is required to be sent from the local unit to the remote unit on another port such as Port 3 or Port 4. These patterns are always available for another process to use, that is, for the ADD data multiplexer 148 to use. A background software task always updates the registers and keeps track of when the tones

and patterns are valid for later use by the ADD data multiplexer 148.

The frequency synthesizer 310 is shown in Fig. 11. The frequency synthesizer 310 receives a base clock frequency as an input and also receives a signal from the microprocessor 300. The frequency synthesizer 310 produces output clock frequencies in 8-kHz increments, from 56 kHz to 1536 kHz. The frequency synthesizer 310 also includes a frequency divisor.

The input to the synthesizer 310 is a base frequency and it uses this base frequency to generate an output to the clock frequency which is then allowed to go into the 4-port clock distributor 150, and is the input called synthesized frequency. This is actually implemented in the frequency synthesizer 310.

Fig. 11 also shows the inputs to the synthesizer 310 received from the microprocessor 300, which determine what value of clock frequency is output. This has a much greater "granularity" than the frequency shown in Fig. 7 for the clock distributor 150, and the frequency synthesizer 310 can be used to generate any 8-kilohertz frequency from 56 kilohertz to 1536 kilohertz. With a different time base, the limits can be adjusted further. The concept would remain the same, i.e., the processor determines the frequency and the synthesizer 310 of Fig. 11 can divide the base frequency by a chosen number to get the output of the clock frequency.

The signalling capture element 240 includes a plurality of signalling registers, as shown in Fig. 12. T-1 NI DROP signalling

data enters at the top left register 241. A status register is maintained as well, as seen in Fig. 12.

In Fig. 12, the signalling is an indication from the switch of the on-hook or off-hook status. It shows 24 bits in 3 separate 8-bit registers. When the signalling bits are valid, they are captured and placed in these registers and then read by software. The software causes a table to be stored in memory of the signalling bits for each channel as they appear from the network. After a call has been placed, the significance of these is that a bit that is equal to zero means that a remote site or a remote unit has not answered the call. If a bit at a particular channel is 1, that means that a remote unit has answered a call. In the same way, if a unit sees a signalling bit equal to one from the switch and it is a unit that has not dialed, it indicates that another unit is attempting to call in to it, and it would then go off-hook toward the switch just as a person would pick up a receiver of a telephone to complete a call. This is the method that is used to get the signalling from the network into the register that can be read by the microprocessor.

In Fig. 12, the status register indicates when the bits are valid, that is, in telephony D4 framing, using robbed bit signalling, the signalling bits to tell the on-hook and off-hook states are valid only in every 6th and 12th T-1 frame and the bits in the status register would be read every frame by the CPU 300 under direction of software. When the proper bits are active in the status register, that would be an indication that all of the

signalling bits 1-24 are valid. There are other bits in the status register that indicate whether frames 6, 12, 18, or 24 are present, and they are also used and recorded along with the signalling bits.

The data capture element 250 is shown in detail in Fig. 13, and receives T-1 NI DROP data at a shift register 251. The shift register 251 supplies an output signal to a channel data sample element 252. The channel data sample element 252 serves as a channel data register. A channel counter 254, which is a divide-by-24 channel counter, supplies one input to a comparator 253. A channel number register 255 supplies the other input to the comparator 253. The comparator 253 then supplies an output signal to the channel data sample element 252.

Fig. 13 represents the data capture section. The data capture is used to capture sequential data from a specific channel. This is used during call setup to let specific patterns that may be received by a remote unit from a sending unit, to perform functions such as synchronization and loopback. The data capture is set up initially with the channel for which the data needs to be captured. This is in the channel number register 255. The microprocessor 300 loads register 255 with the channel number, for example channel 5.

A counter 254 is incremented every time a channel's data is valid. This counter increments from 1 through 24 and then repeats each T-1 frame. A comparator 253 shown in Fig. 13 compares the channel number written by the microprocessor 300 in register 255 with the current count that is valid at that particular time from the counter 254. When the comparator determines that the two are

the same, it then will store the current data that is valid at the particular compare time, in this example channel 5.

When those two are compared equal by the comparator 253, then the data that is then captured or available in the shift register 251 is then written to a channel data sample register 252. The register 252 is then available for the microprocessor 300 to read, and it represents an 8-bit sample from (in this example) channel 5, which was captured from the network from the T-1 telecommunications line on that channel 5. The CPU under direction of the software has an opportunity to read this, every T-1 frame, that is every time channel 5 data becomes available. The software can then load an array, which can be a very long array, with consecutive samples from a particular channel.

Once the software array has been loaded with data, it can be inspected for messages and patterns sent from a remote dialing inverse multiplexer. The messages and patterns may include loopback requests, phone numbers, internal configuration parameters, and synchronization information.

The shift register 251 is simply a serial-to-parallel shift register. Since the data coming from the network is in a serial bit stream, the shift register allows 8 bits to be captured at a particular time. It is always being updated bit-by-bit. Therefore, when the channels are compared equal, then at that precise moment the contents of the shift register 251 are then transferred and locked into the channel data sample element (register) 252. The contents of the element 252 then do not change

until the next T-1 frame, whereas the element 251 will then continue to be updated with other channel data that is not of concern at the present time. The CPU under control of software then has an entire T-1 frame time to read the register 252 without risk of it being updated for another 125 microseconds, which is the time for a T-1 frame using D4 framing.

Fig. 14 schematically shows the synchronizer 280 of Fig. 5, having a shift register 281 which receives T-1 serial data, a delay equalization buffer 282 receiving the output of the shift register 281, and an output shift register 283 which receives data from the delay equalization buffer 282 as input. The shift register 283 outputs synchronized serial data. The delay equalization buffer 282 allows storage of T-1 data for 340 milliseconds, and receives the output of the shift register 281 at a port DI, and outputs data to the shift register 283 at a port DO. The delay equalization buffer 282 has ports AI and AO which respectively receives inputs from an address counter 284 and an adder 286.

The address counter 284 supplies an incrementing 16-bit address, both to the port AI of the delay equalization buffer 282 and to the adder 286. The address counter 284 also supplies a second output signal, which is a divide-by-24 index, to delay registers 285. The output of the delay registers 285 is supplied as an input to the adder 286. The added signals from the adder 286 are then supplied to the delay equalization buffer 282.

The shift register 281 is a serial-to-parallel shift register. It receives serial data from the T-1 telecommunications line,

converts it to 8-bit parallel data and is supplied to the buffer 282 as a data input. The shift register 283 operates in just the reverse fashion. The shift register 283 takes 8-bit parallel data and shifts it bit by bit so it becomes serial again. The output of this shift register represents serial synchronized data; the replica of the data as it was transmitted at the remote dialing inverse multiplexer.

The buffer 282 is a 2-port memory that will accept data input (DI) and will accept address input (AI) as viewed in Fig. 14. Then, data is output at DO according to the AO input. The buffer 282 is able to store samples of data captured from the T-1 telecommunications line, and its storage capacity is selected to be of a size that represents approximately 340 milliseconds of data, before old data is overwritten by new data. The entire buffer memory can be thought of as a circular memory of samples from the T-1 telecommunications line which will be overwritten in approximately 340 milliseconds. The buffer memory size can be increased for specific applications, however the basic concept remains the same.

The address counter 284 shown in Fig. 14 is used for two purposes. The first is to address the buffer 282 and the second is to address the delay registers 285. The registers 285 contain a 16-bit delay offset for each channel and this offset represents the relative network delay between the channel with the fastest route and the channel indicated. The relative network delays are determined during the synchronization process (described elsewhere

in this document) and are written by the microprocessor 300 into these registers. The adder 286 is a 16-bit adder which will add the address from the address counter 284 and the 16-bit delay offset from the register 285 which is indexed by the divide-by-24 counter. The resulting 16-bit address is used to read from the buffer 282. The elements shown in Fig. 14 represent a hardware solution for synchronizing 56 kilobit and 64 kilobit data. Once the network delays have been determined and the relative delay between channels has been stored in the delay registers 285, no further updating is necessary; that is, the address counter 284 runs freely and the resisters 285 contain all the synchronizing information necessary to reconstruct the data stream as it appeared at the transmitting remote dialing inverse multiplexer. The elastic store/DROP element 180 is shown in Fig. 15 as including four identical elastic store elements 181-184. Each of the elastic stores 181-184 respectively receives clock/data from ports 1-4. The function of the elastic stores 181-184 is to receive clock/data which is in the form of bursts (as indicated to the left of elastic store 181 as a "burst clock in signal") and to output the received clock/data signals in a smooth, regular manner. That is, the average rate of data going into the elastic stores 181-184 will be equal to the average data rate going out of elastic stores 181-184. The purpose of using the elastic stores 181-184 is to smoothly regulate the flow of data through the loopback controller 190 and to the 4-port V.35 drivers 120. The CPU 300 is connected to the elastic stores 181-184, in order to provide overflow detection,

underflow detection, a manual input clock, and a manual output clock.

The elastic store has a very simple function. It takes clock and data on the input side, and delivers a smooth clock and data on the output side. The elastic store is known in the art. The elastic store element simply smooths the clock to provide an even duty cycle of clock and data on the output side. The frequencies are identical from the input to the output, otherwise data would be lost or overwritten, and that is one of the functions of the elastic store. The elastic store does have the ability to detect overflows and underflows and these status bits are presented to the microprocessor for error checking. Also, the microprocessor 300 can manually load the elastic stores to initialize them before they are actually used. This is important to keep the elastic store half full when possible so that lead changes can be accommodated easily. This will prevent overflows and underflows.

The elastic store/ADD 170 is shown in Fig. 16 and includes a plurality of elastic store elements 171-174. The elastic store/ADD 170 operates in a manner similar to that of the elastic store/DROP 180 in that it receives data from respective ports 1-4, but in which data is received in a smooth, regular manner and is output in bursts. The output data is sent to the T-1 ADD data multiplexer 148. The CPU 300 provides overflow detection, underflow detection, a manual input clock, and a manual output clock.

@@ The elastic store 170 of Fig. 16 is substantially the same as described previously with regard to Fig. 15, except used on the ADD

side instead of the DROP side. All the overflow and underflow detection bits are the same as they were for the DROP elastic stores of Fig. 15. Also, the elastic stores can also be loaded and initialized to the half full state to prevent overflows and underflows.

The ADD data multiplexer 148 includes a plurality of data source ports 148a, 148b, 148c, and 148d, as shown in Fig. 17. The outputs of the data source ports 148a-148d are supplied to a multiplexer 149a. Data source selection registers 147 include port selection elements which supply port selection signals to respective data source ports 148a-148d.

Inputs to the ADD data multiplexer 148 include data streams bracketed as group "A" representing "ADD" data for each of the ports, and patterns bracketed as group "B" which are common to all data source ports 148a, 148b, 148c, 148d as indicated in Fig. 17. The signals in group "A" can include Port 4 add data, Port 3 add data, Port 2 add data, and Port 1 add data. The signals in group "B" can include DTMF digit patterns, sync pattern, PRBS 511 pattern, a shared messaging pattern, a spare pattern, and PRBS (2e20)-1 pattern. An additional input to the multiplexer 149a is an "expansion in" signal. The multiplexer 149a produces an "expansion out" signal, and supplies the same signal to an input of a multiplexer 149b. The other input of the multiplexer 149b receives T-1 CI DROP data, and the multiplexer 149b outputs T-1 NI ADD data.

The ADD multiplexer shown in Fig. 17 is a series of four individual 8 to 1 selectors 148a, 148b, 148c, 148d whose outputs are then time multiplexed together to form an output data stream which then goes to the network interface (NI). This is the essential part of the drop and insert technology, this being the insert portion. It is on this module that data from other interfaces, called the customer interfaces (CI) downstream from the dialing inverse multiplexer 100, will be added in addition to the data that is generated by the dialing inverse multiplexer 100 toward the network. In element 148 the blocks 148a, 148b, 148c, and 148d have identical functions. They are able to select data from three different sources. The first source in Fig. 148a is port 1 ADD data. This represents the data from the elastic store in this case element 171 which is simply the user data transmitted from the user device (e.g. CODEC) to the dialing inverse multiplexer 100. If, for example, a CODEC is connected to data interface to Port 1, the CODEC's data is presented to the data source port 1 block 138a and if it is appropriate, the software would then allow that data to be added to the NI T-1 data stream by blocks 149a and 149b. Software can also choose to add in DTMF tones, which is Pattern 1 shown in the B collection of inputs, or Pattern 2 which the echo cancel disable tone, or Pattern 3 which is defined as the synchronizing pattern, or Pattern 4 which is the software defined pseudo random bit sequence 511 pattern, or Pattern 5 which is not specifically defined but can be shared among the blocks 148a, 148b, 148c, and d as required. That is true also with

the other inputs of the group B. The group B inputs are common to 148a, 148b, 148c, and 148d. The signal port 1 ADD data in group A under is presented only to element 148a and Port 2 ADD data is only presented to element 148b, etc.

The element 149a combines the outputs from blocks 148a through 148d and also any expansion inputs which may be implemented in the future. It will combine these to form a bit serial data stream which will then go to block 149b to be added to the NI T-1 data. The signal going to 149b called expansion out can also be used for future expansion, in which case the expansion out of the dialing inverse multiplexer 100 would become the expansion in of another dialing inverse multiplexer 100. This provides a method of cascading inverse multiplexer logic together to provide multiple ports, more than 4, as shown here. The data source selection registers 147, determine which of 8 possible inputs to the data source multiplexers is to be selected as input to the multiplexer 149a. The selection is made by software and this selection will change during call setup. For example during a call set up on port 1, the first data selected to the T-1 would be the DTMF digits, that is, Pattern 1 of group B. After the digits have been presented to the network switch and software then determines if the remote dialing inverse multiplier has answered, it will then change the selection from Pattern 1 to Pattern 2, which is an echo canceler disable tone used to disable any echo cancelers which are present between switches in the network. Software then selects Pattern 3, the synchronizing pattern, to be transmitted on all

connected channels. After synchronization and network delays have been determined, software will select the Port 1 add data to the network interface, allowing user data to be transmitted through the network to the remote dialing inverse multiplexer.

Fig. 18 schematically shows the loopback controller 190 depicted in Fig. 5, having elements 194-196. The elements 194-196 respectively receive output signals from a remote loopback 191, local loopback 192, and V.25 bis data element.

Fig. 19 is a flow chart similar to Fig. 4, indicating operation of the local dialing inverse multiplexer 100 as it would be used to communicate with a remote dialing inverse multiplexer 100', where the local dialing inverse multiplexer 100 has a 24 channel capacity. The sequence of steps is the same as that shown in Fig. 4, and like blocks have like functions. Blocks 512', 514', 515', 516', 517', 518', and 524' differ from the embodiment shown in Fig. 4 in that 24 channels are specified, and N represents the 23 additional lines (i.e., beyond the first line, which was used to initiate the communication).

In Fig. 21, the synchronizing pattern should be able to equalize relative channel delays of 340 milliseconds. A counter which is incremented each T-1 frame, 125 μs, must therefore have at least 2720 counts. For the receiver to make adjustments, the count must be doubled to 5440 counts. This number of counts, 5440, requires 13 bits (2^{13} = 8192) which can be transmitted over 3 frames as follows using 5 bits in each frame:

7	6	5	4	3	2	1	0
0	<--LSB---->						1
1	<--MSB---->						1

The synchronizing pattern consists of triads which encode a decrementing 15-bit count as follows:

Bit:	7	6	5	4	3	2	1	0
A	0	1	P14	P13	P12	P11	P10	1
B	1	1	P9	P8	P7	P6	P5	1
C	1	1	P4	P3	P2	P1	P0	1

In the above table, A represents a high order pattern byte, B represents a middle order pattern byte, C represents a low order pattern byte, elements P0-P14 represent the 15 bit sync pattern, and the leftmost bit (under the heading 7 in the above table) represents a triad identifier. In this example, a 15 bit pattern will accommodate a $2^{(15-1)} \cdot 125\ \mu$sec delay (= 2 sec).

In Fig. 23, A is a bit sync pattern encoded in each triad. Once each T-1 frame, 1/3 of the triad is transmitted. Every third T-1 frame, the pattern contents are decremented. The transmitter places this synchronizing pattern onto all channels which require synchronization. The receiver captures a sample of data from all channels to be synchronized and determines the network delay by comparing the pattern count from channel to channel. In Fig. 23, it is assumed that 3 channels are used.

The received data of the example of Fig. 23 would appear in memory as shown in Fig. 24. For this example, the data is present in the address registers as shown in Fig. 25.

The synchronization is done in software, as part of the sequence shown in the flowcharts of Figs. 4 and 19. One key advantage of the synchronizing algorithm used is that only 5 • (channel bandwidth) bytes are required for the software to determine network delays. The number 5 comes from (2 • 3 {triad}) - 1). The algorithm first determines the offset to the beginning of the triad (byte A) for each channel. It then captures the triad (three bytes) and finds the lowest number among all channels. From this base, the relative offsets of the other channels are computed.

In the foregoing example, the triad for channel 1 starts at ADDR = 0, 9, 12; the channel 2 triad starts at ADDR = 4, D, 16; and the channel 3 triad starts at ADDR = 8, 11, 1A. Therefore, the initial offsets for channels 1-3 are 0, 4, 8. The triad number is extracted from the address mentioned, as follows:

Channel 1: ADDR 0, 9, 12 = triad number 5

Channel 2: ADDR 4, D, 16 = triad number 3

Channel 3: ADDR 8, 11, 1A = triad number 4

The lowest triad number among the three is from channel 2, which has the least network delay. From this base, channel 1 has a relative offset of 2 while channel 3 has an offset of 1. These relative offsets are multiplied by three (3 = number of bytes per triad) multiplied by the number of channels = 3, and added to the initial offsets to yield the resulting offsets shown in Fig. 26 for channels 1-3.

Fig. 28 illustrates another embodiment of the device shown in Fig. 5, in which an RS-232 modem 701 is connected for communication with the CPU 300, to enable remote control by telephone of the remote dialing inverse multiplexer 100'. The modem 701 permits operation of the remote dialing inverse multiplexer 100' from a distant site, including all operations which could ordinarily be performed using the keyboard at the remote dialing inverse multiplexer 100'.

The other numerals shown in Fig. 28 which are the same as those in Fig. 5, have the same description and function substantially the same as described above with respect to the embodiment of Fig. 5.

It will be understood that the above description of the present invention is susceptible to various modifications, changes and adaptations, and the same are intended to be comprehended within the meaning and range of equivalents of the appended claims.

WHAT IS CLAIMED IS:

1. An apparatus for data communication, comprising:

a first interface means for interfacing with a data communications network;

a second interface means for interfacing with a data source; and

data multiplexing means for multiplexing data from the data source into a selected number of channels.

2. An apparatus as claimed in Claim 1, further comprising automatic dialing means for dialing a chosen number for connection with a remote device.

3. A method for reconstructing data sent from one communication device to another communication device on a predetermined number of telephone lines, comprising the steps of:

sending an alignment packet;

determining channel alignment;

sending a synchronization packet;

determining synchronization; and

reconstructing data transmitted between the communication devices.

4. An apparatus for data communication, comprising:

a first interface means for interfacing with a data communications network;

a second interface means for interfacing with a data source;

data multiplexing means for multiplexing data from the data source into a selected number of channels;

means for selecting the number of bits in a channel for fractional channel usage, depending upon a required data rate.

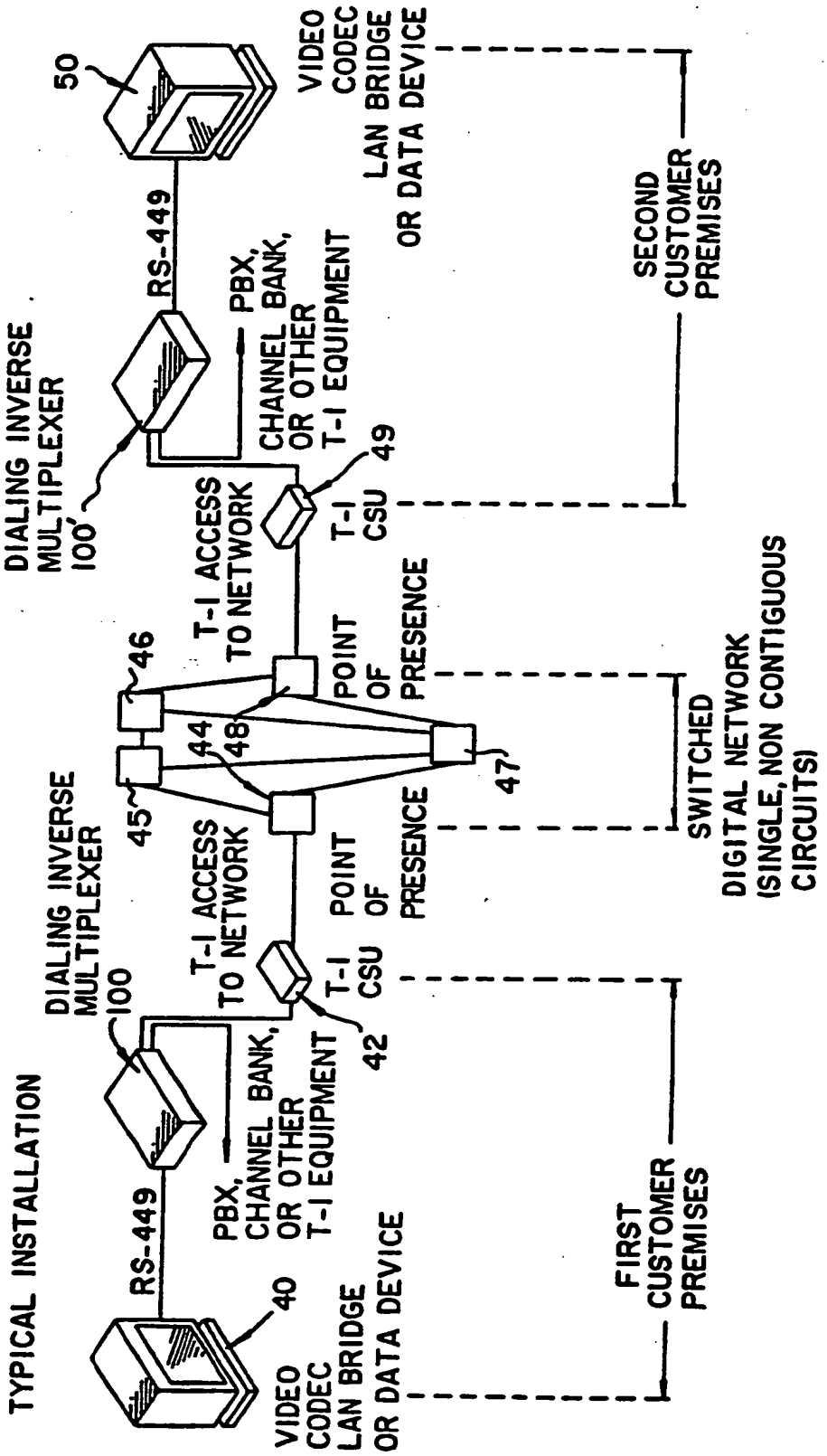


FIG.1

2/39

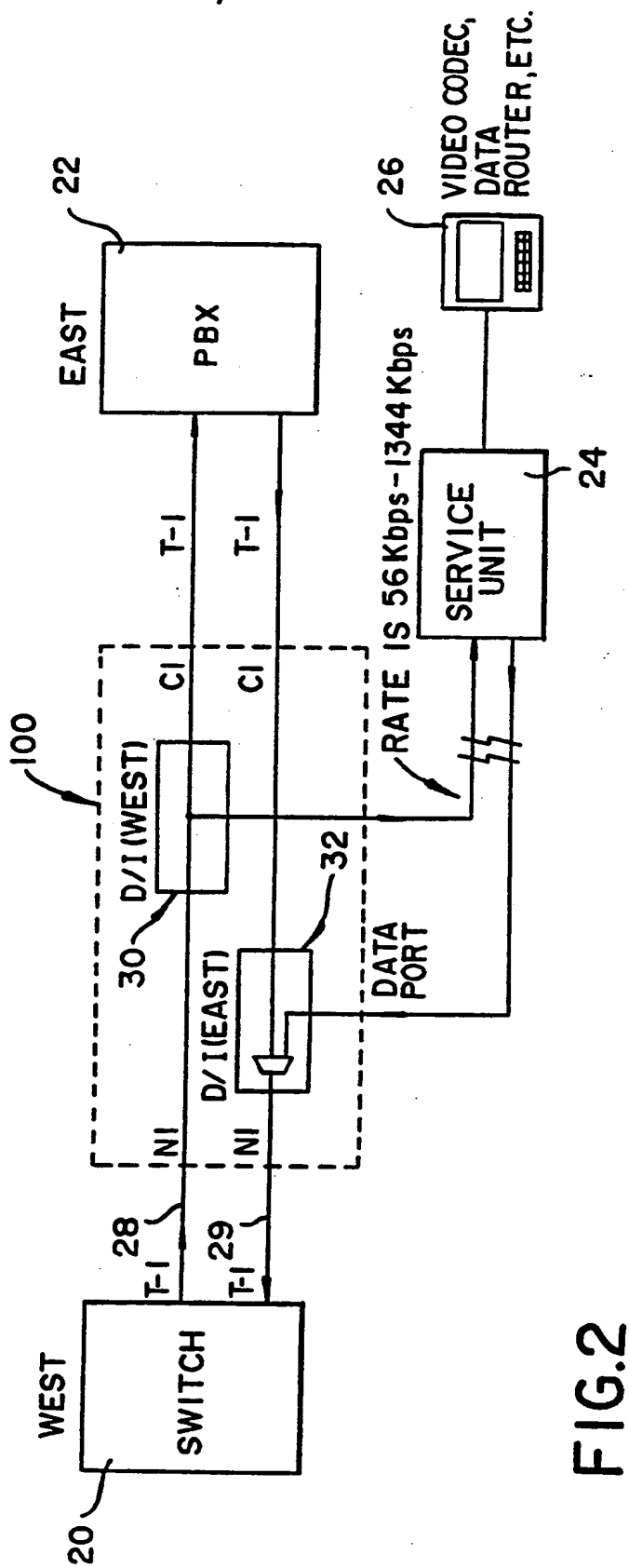


FIG.2

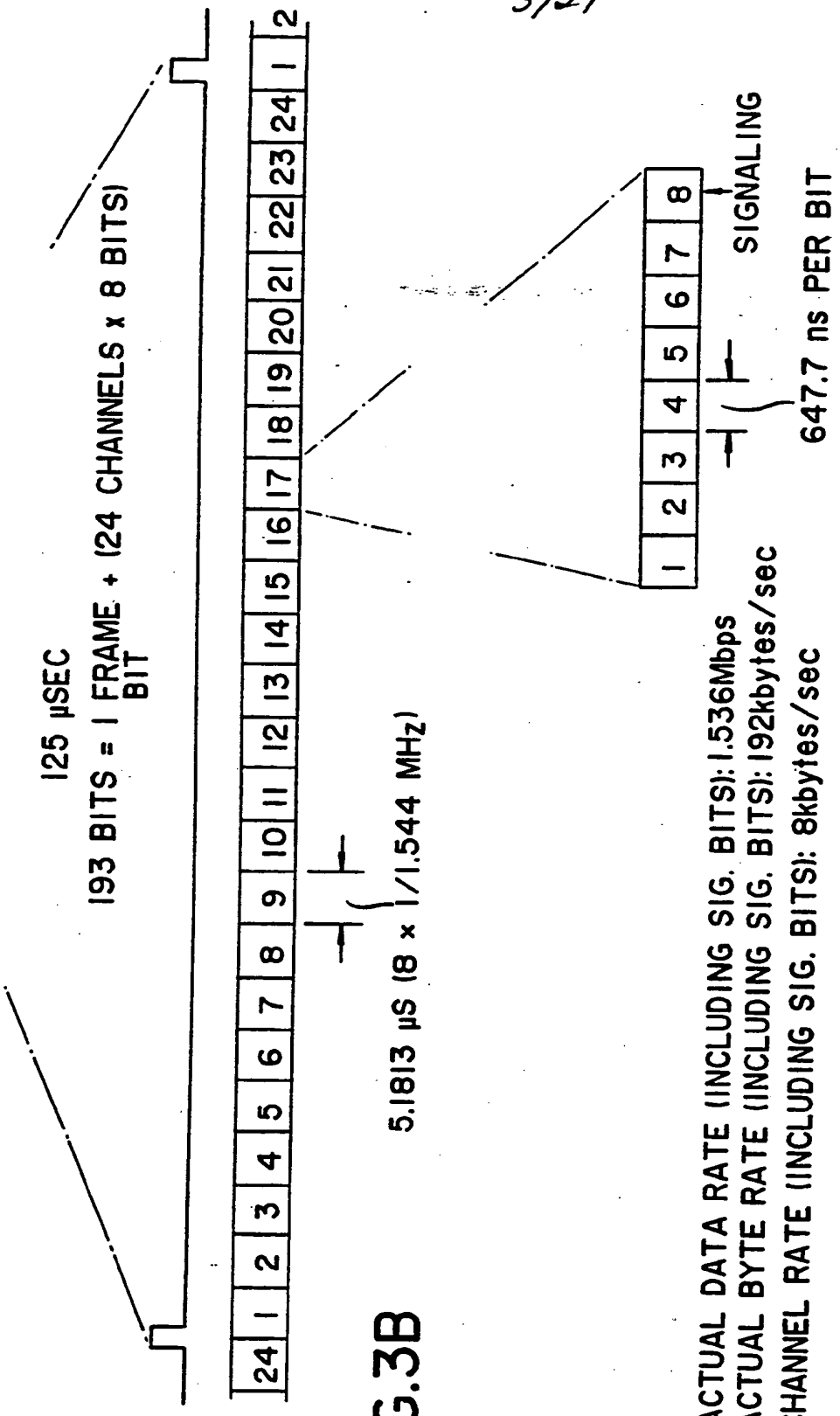


FIG.3B

FIG.3A

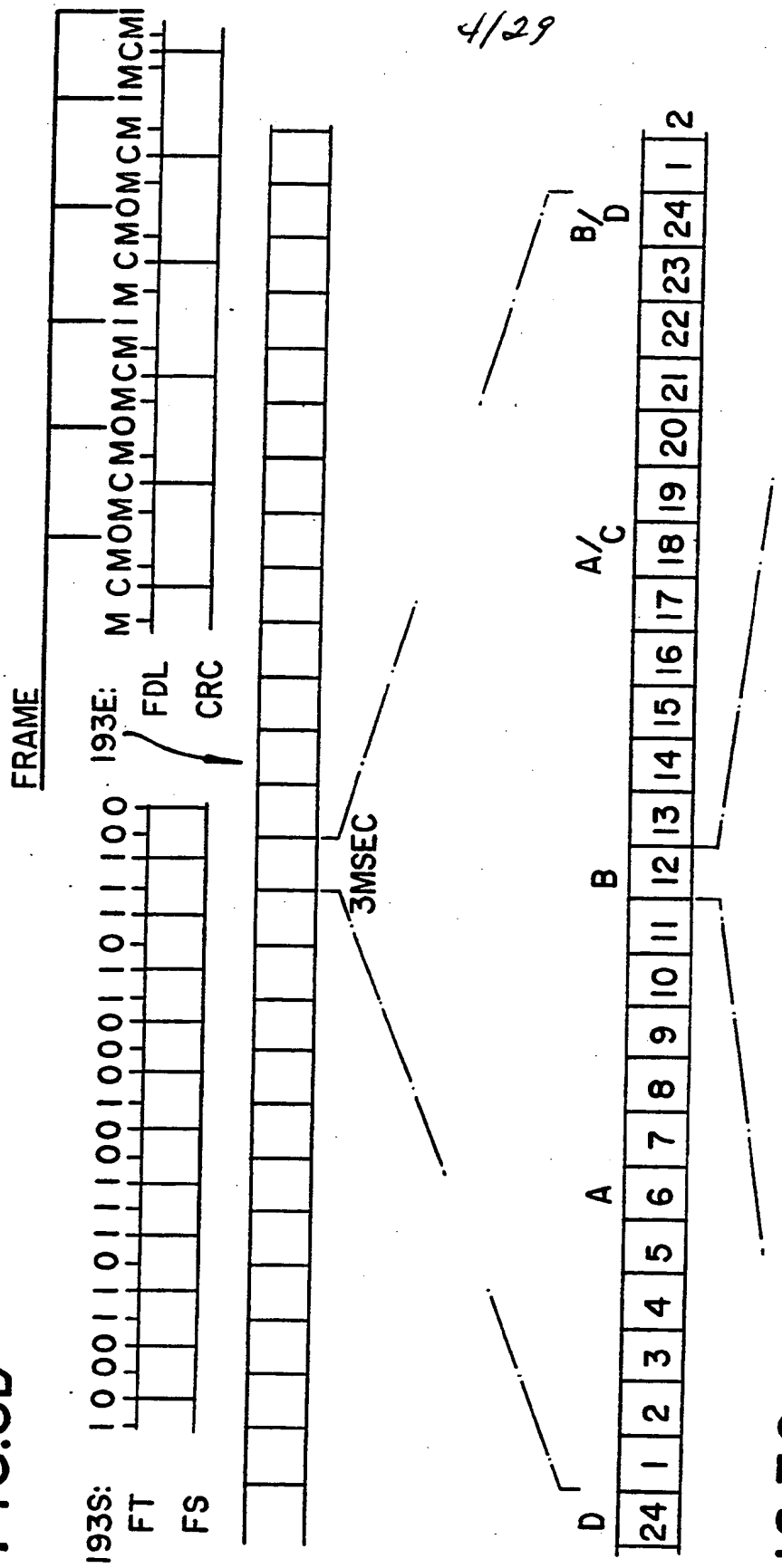
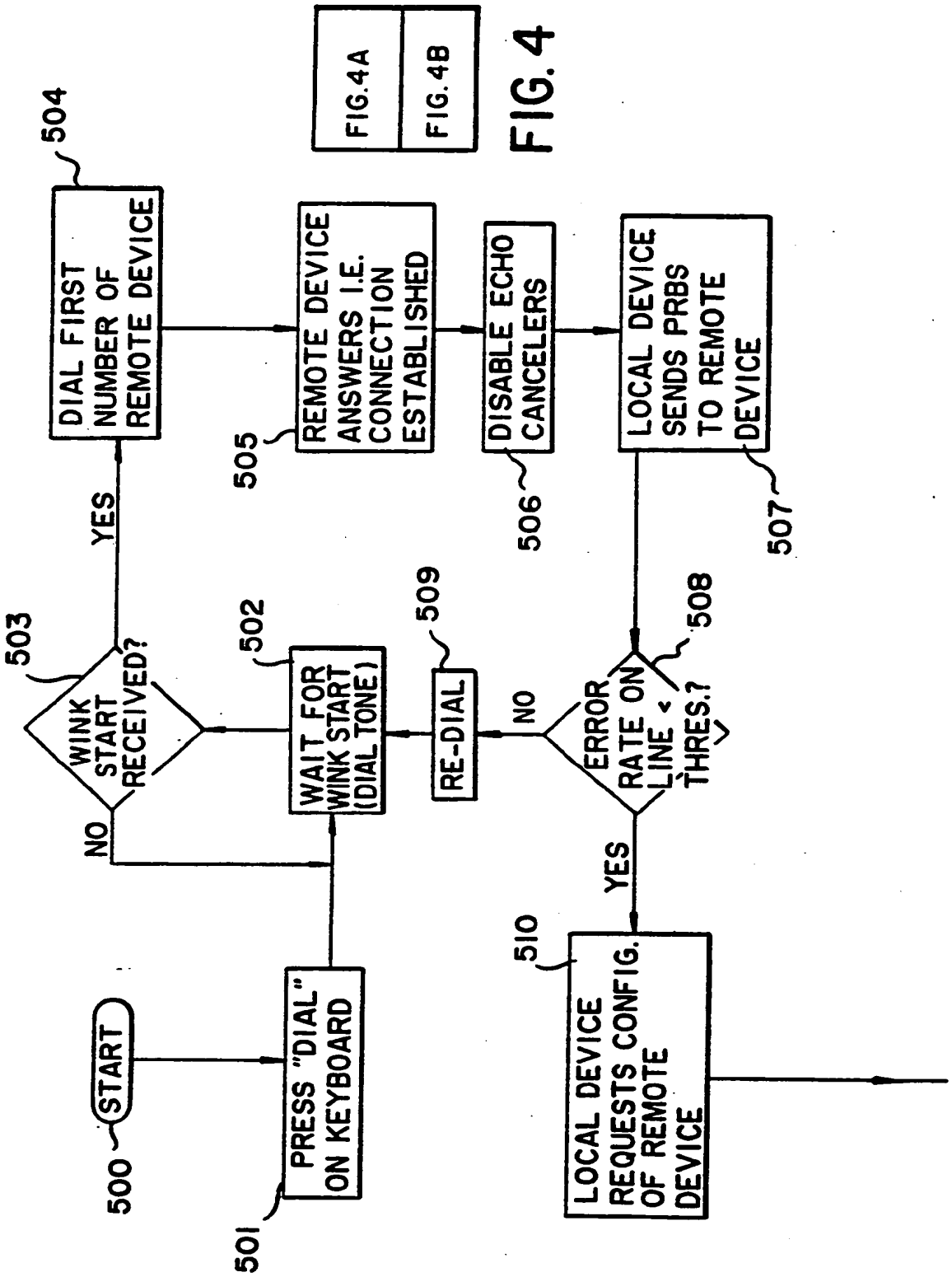


FIG.3D

FIG.3C

5/29



SUBSTITUTE SHEET

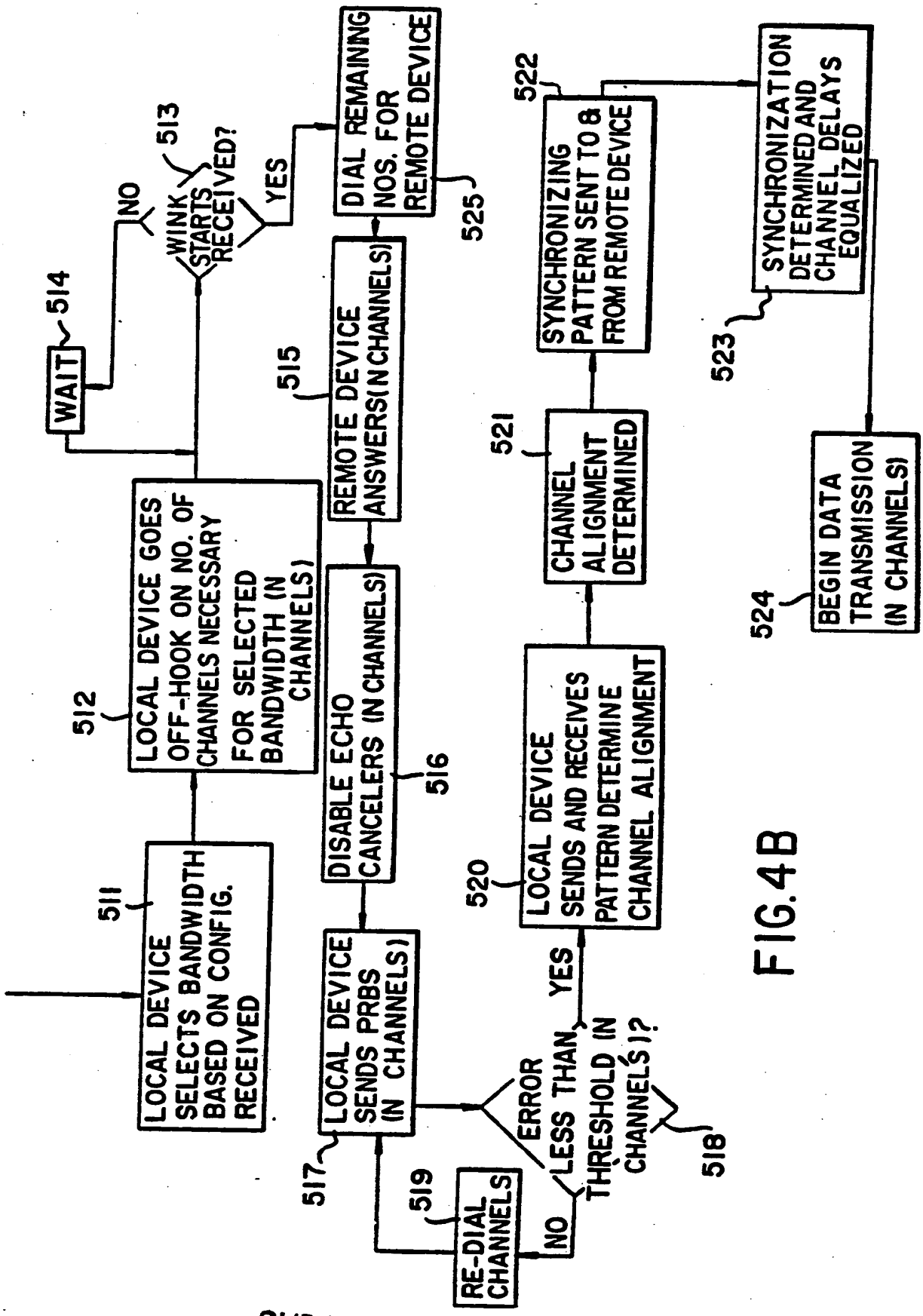


FIG. 4B

FIG. 5

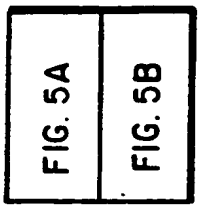
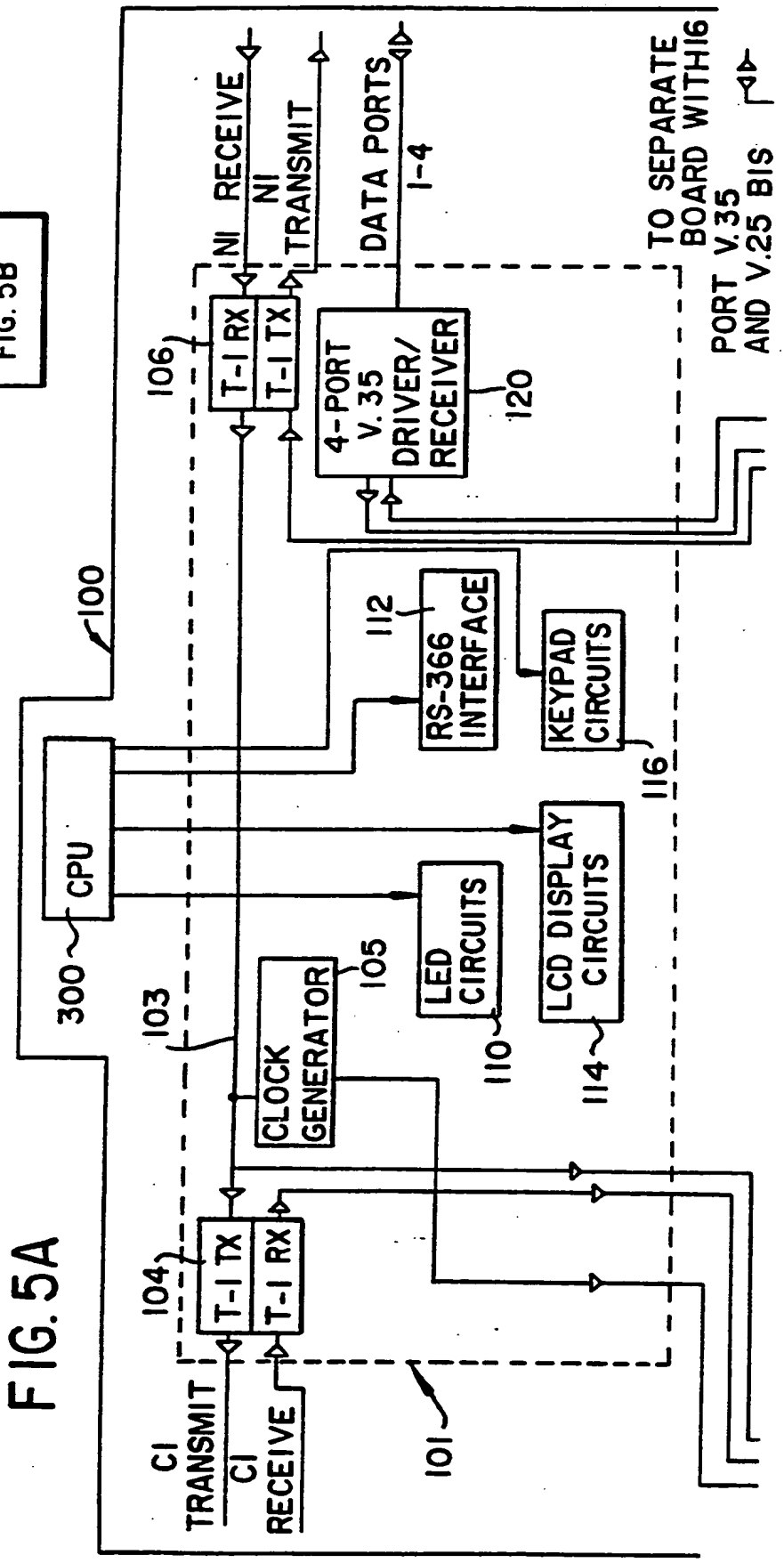


FIG. 5A



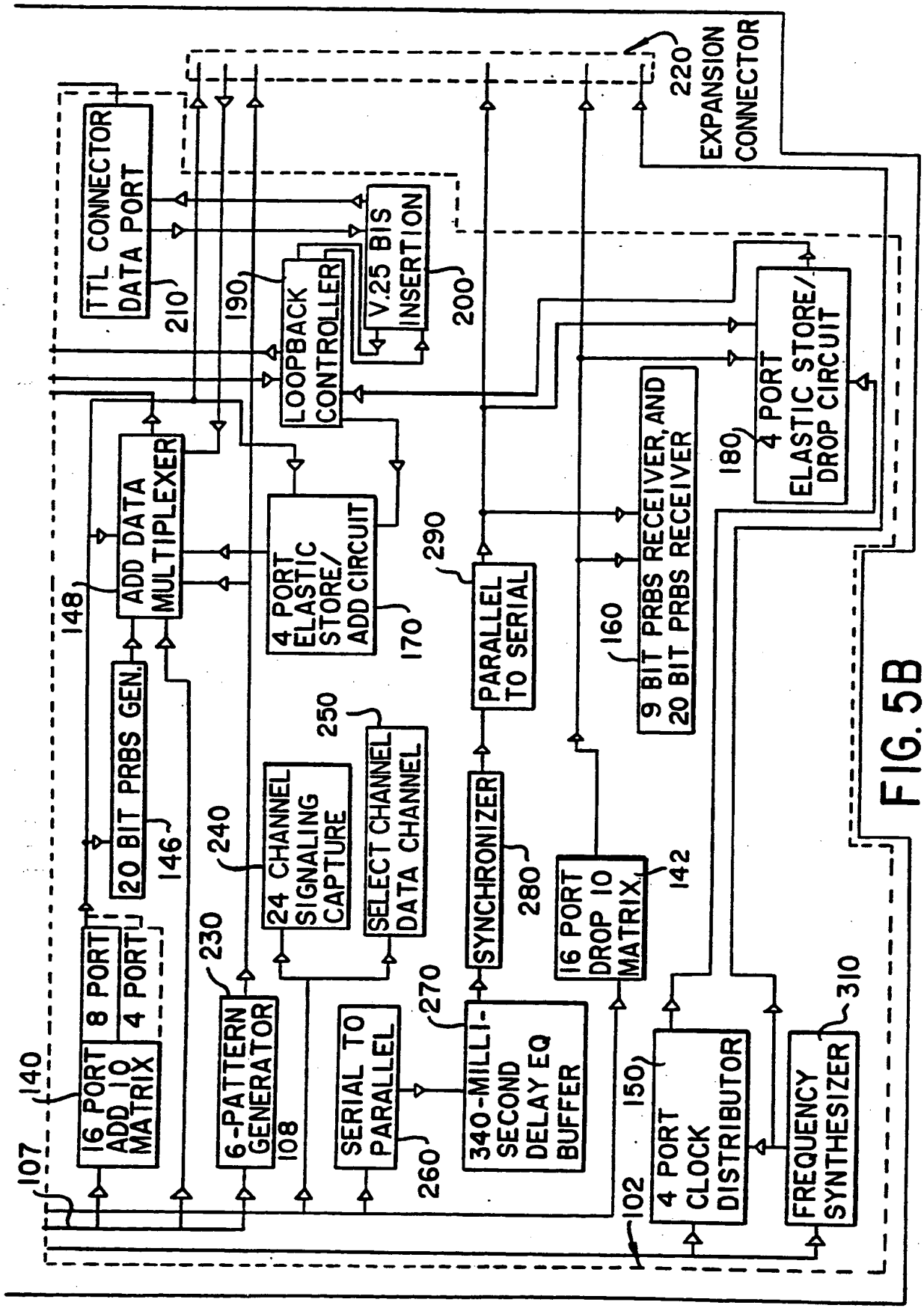


FIG. 5B

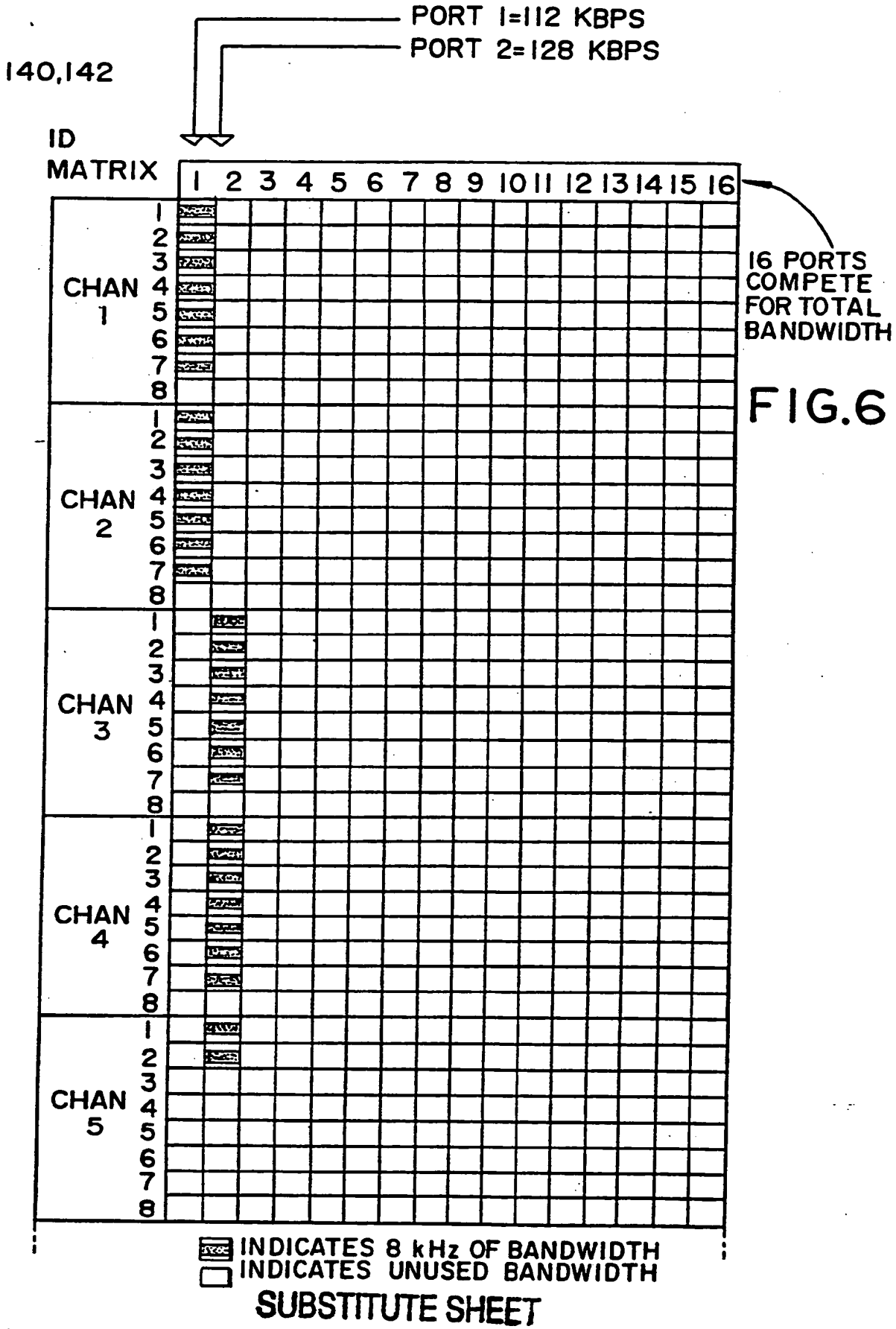


FIG.6

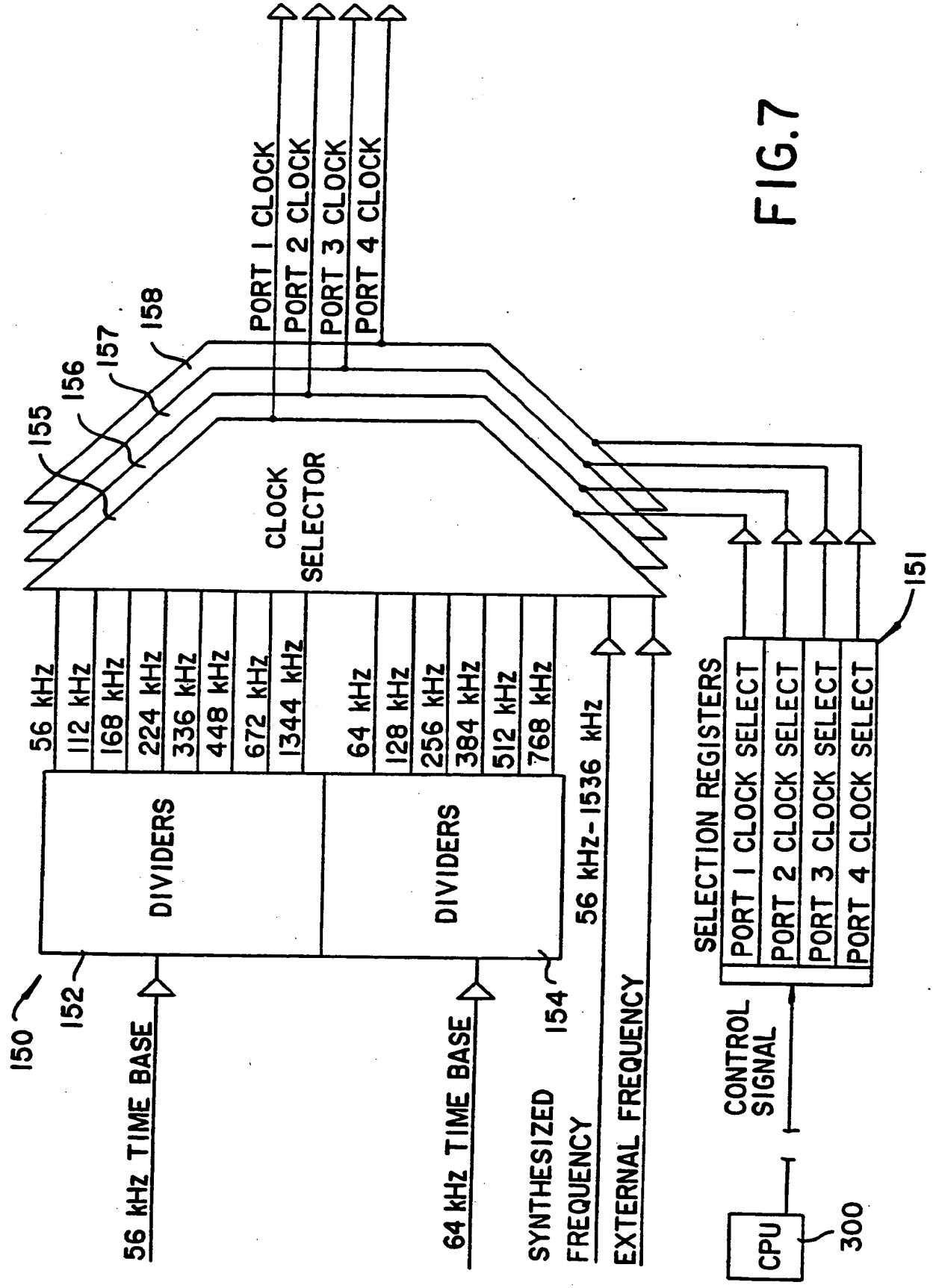


FIG.7

FIG.8

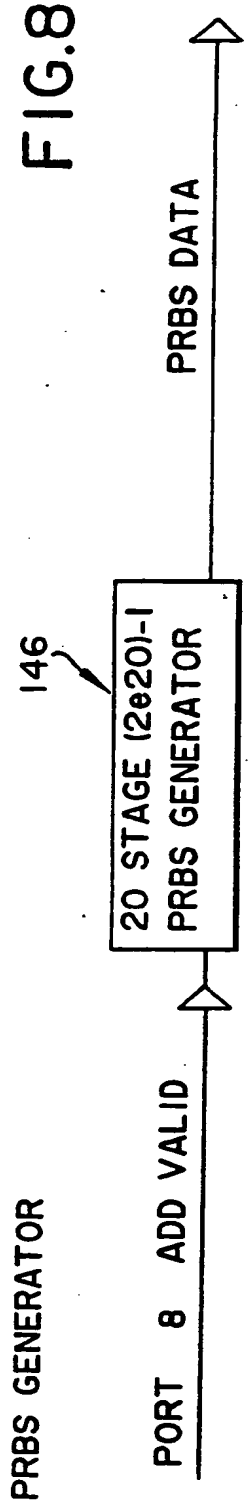
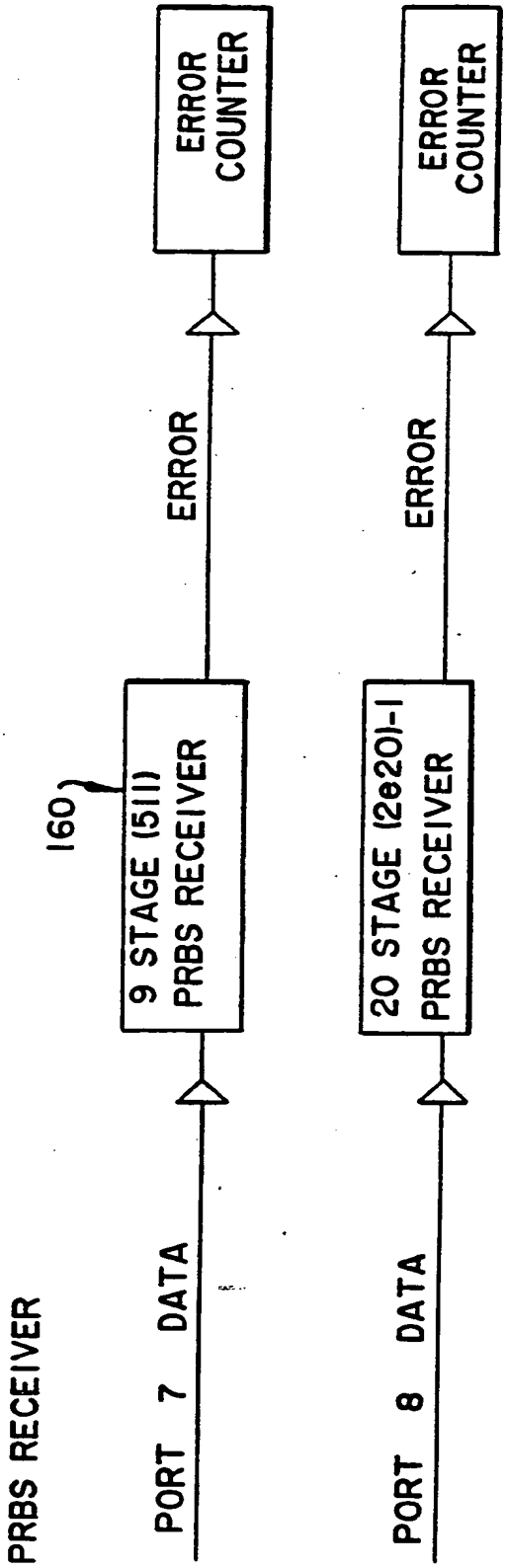


FIG.9



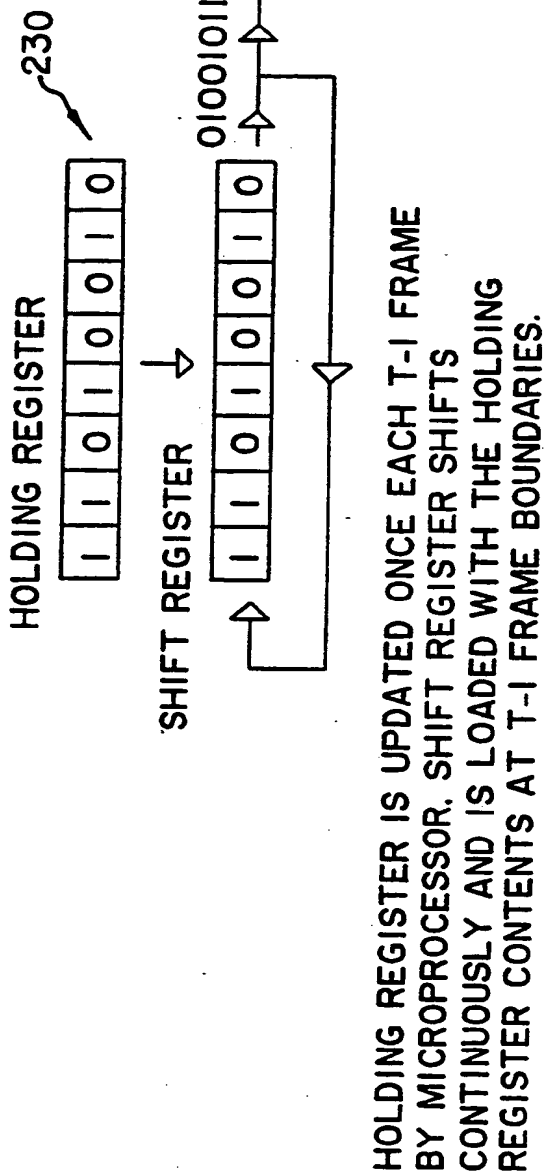


FIG.10

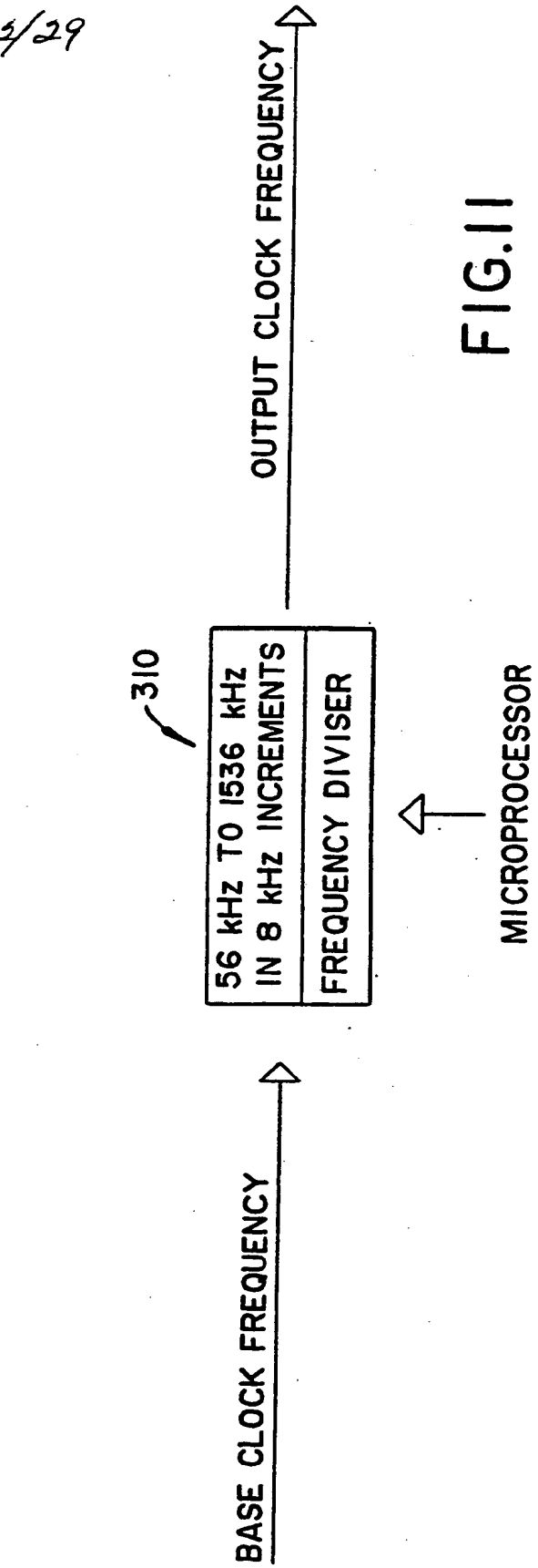


FIG.11

FIG.12

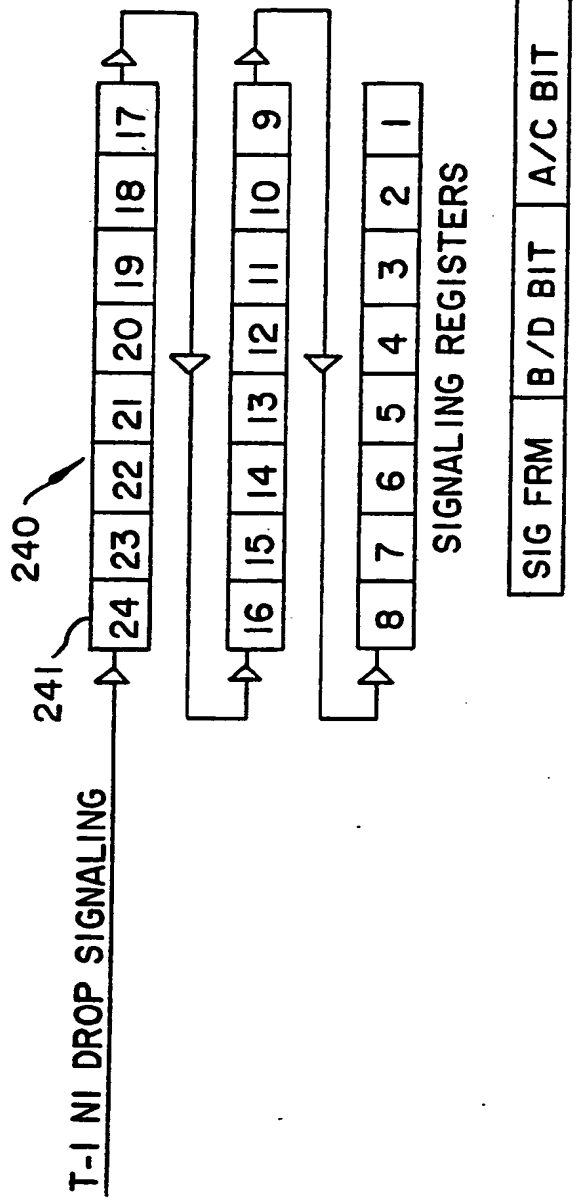
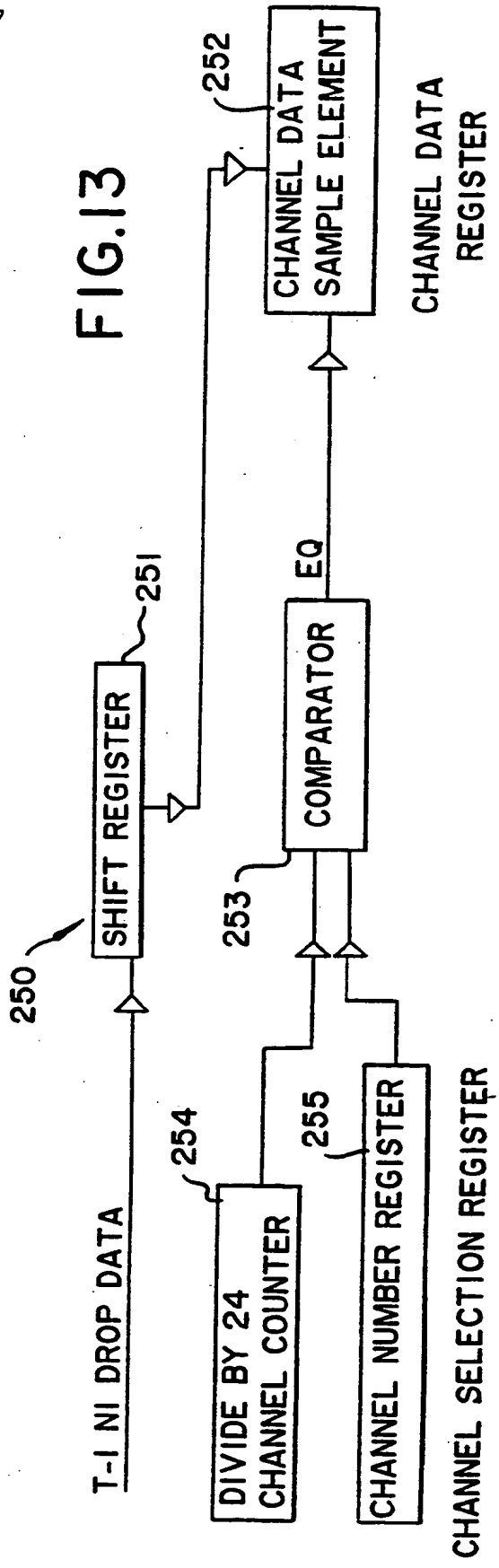


FIG.13



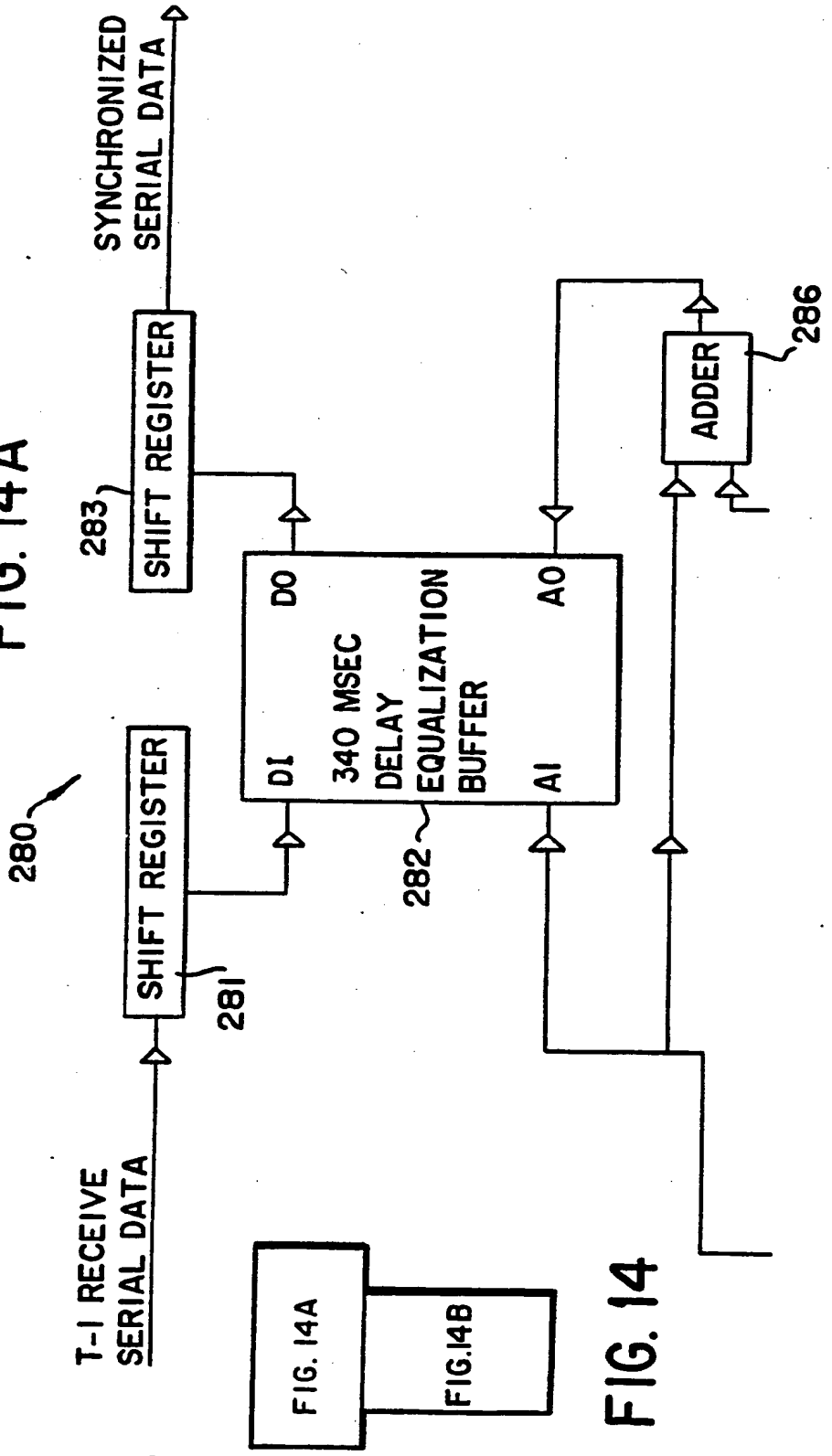


FIG. 14A

FIG. 14

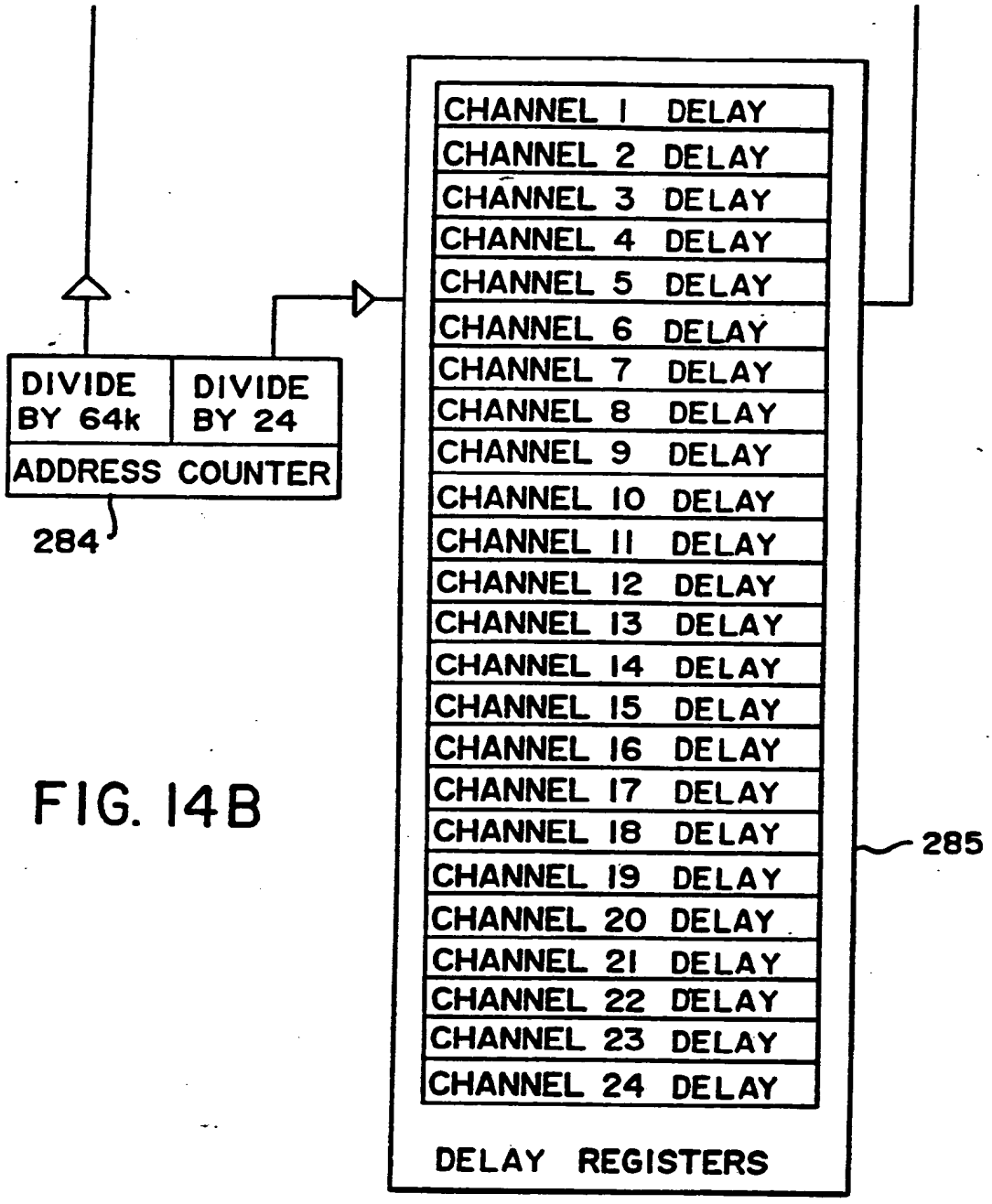


FIG. 14B

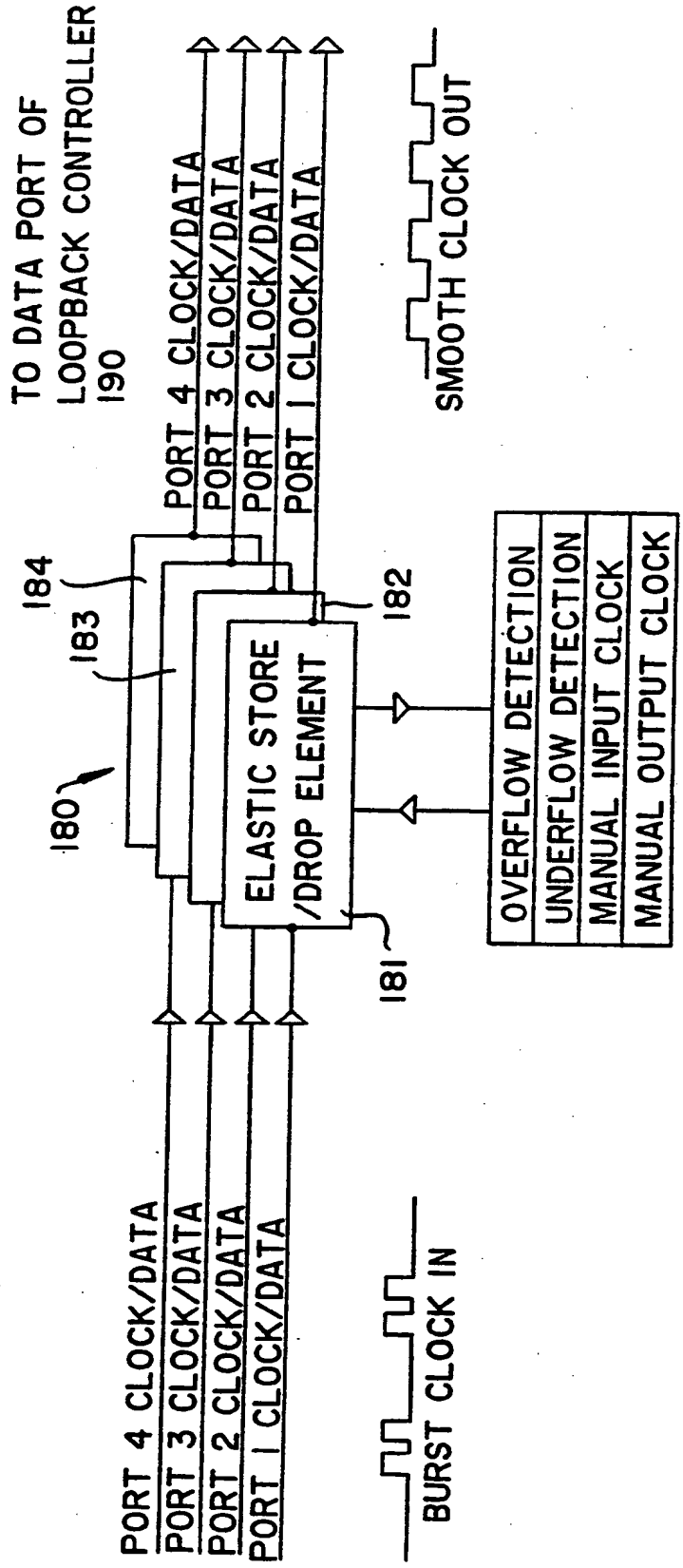


FIG.15

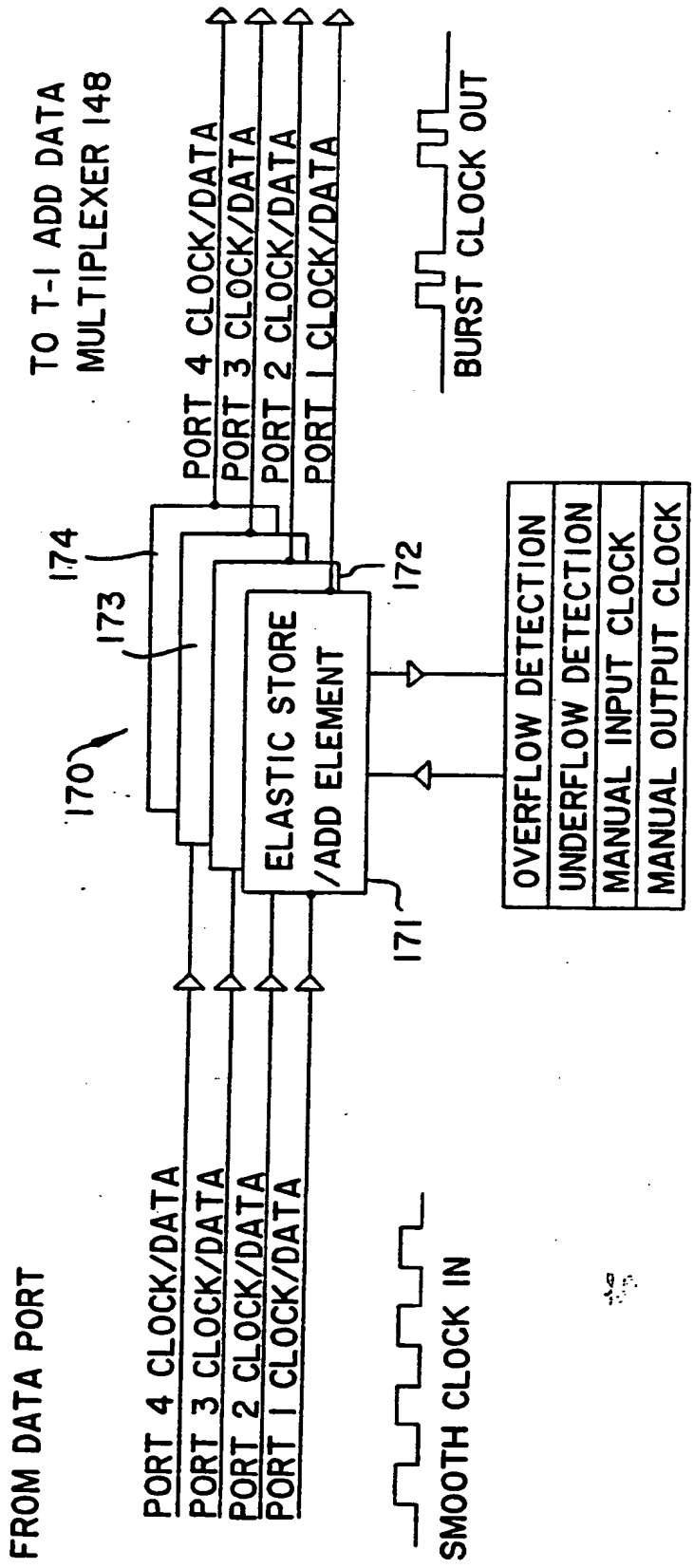
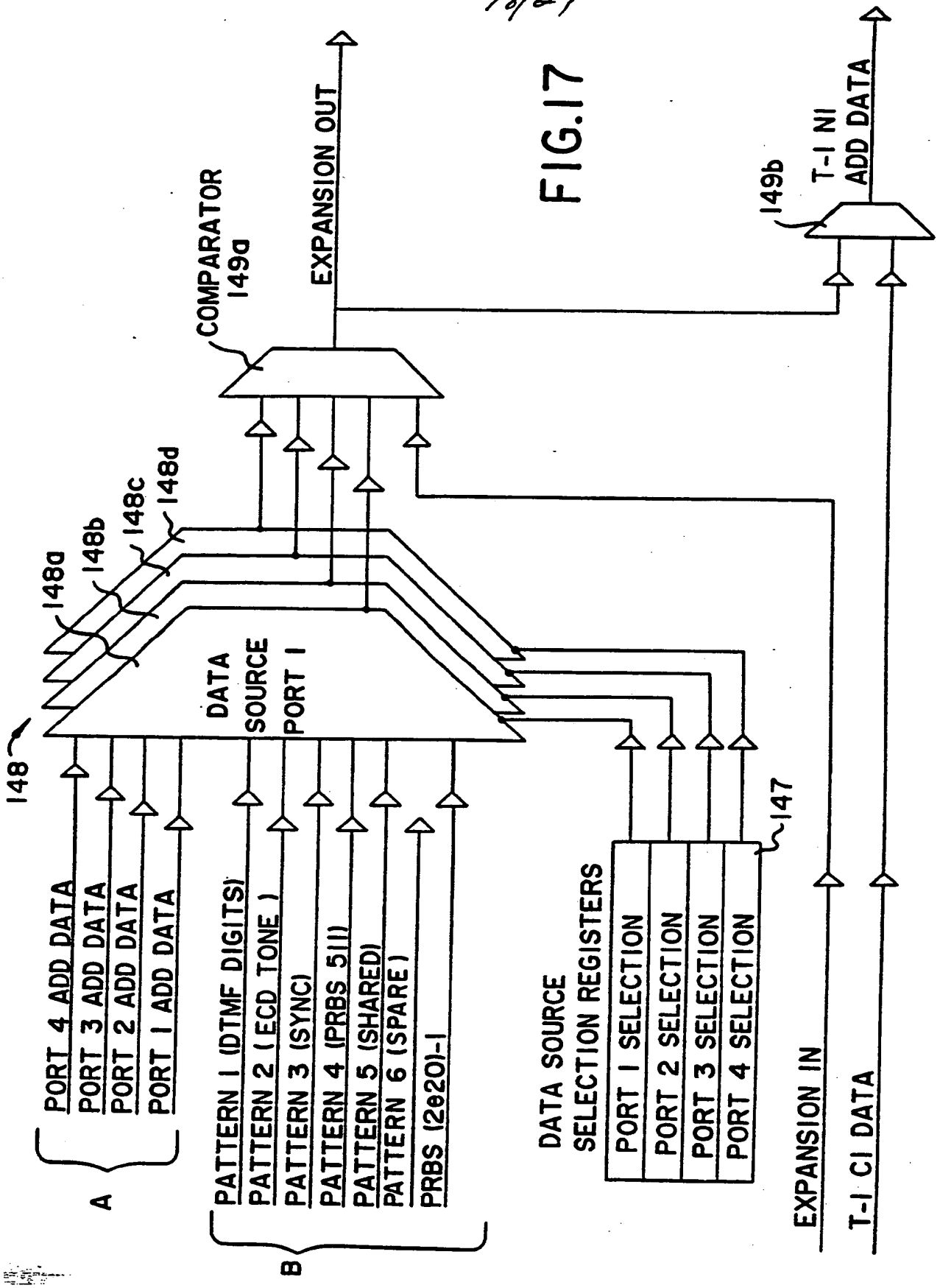


FIG.16

FIG.17



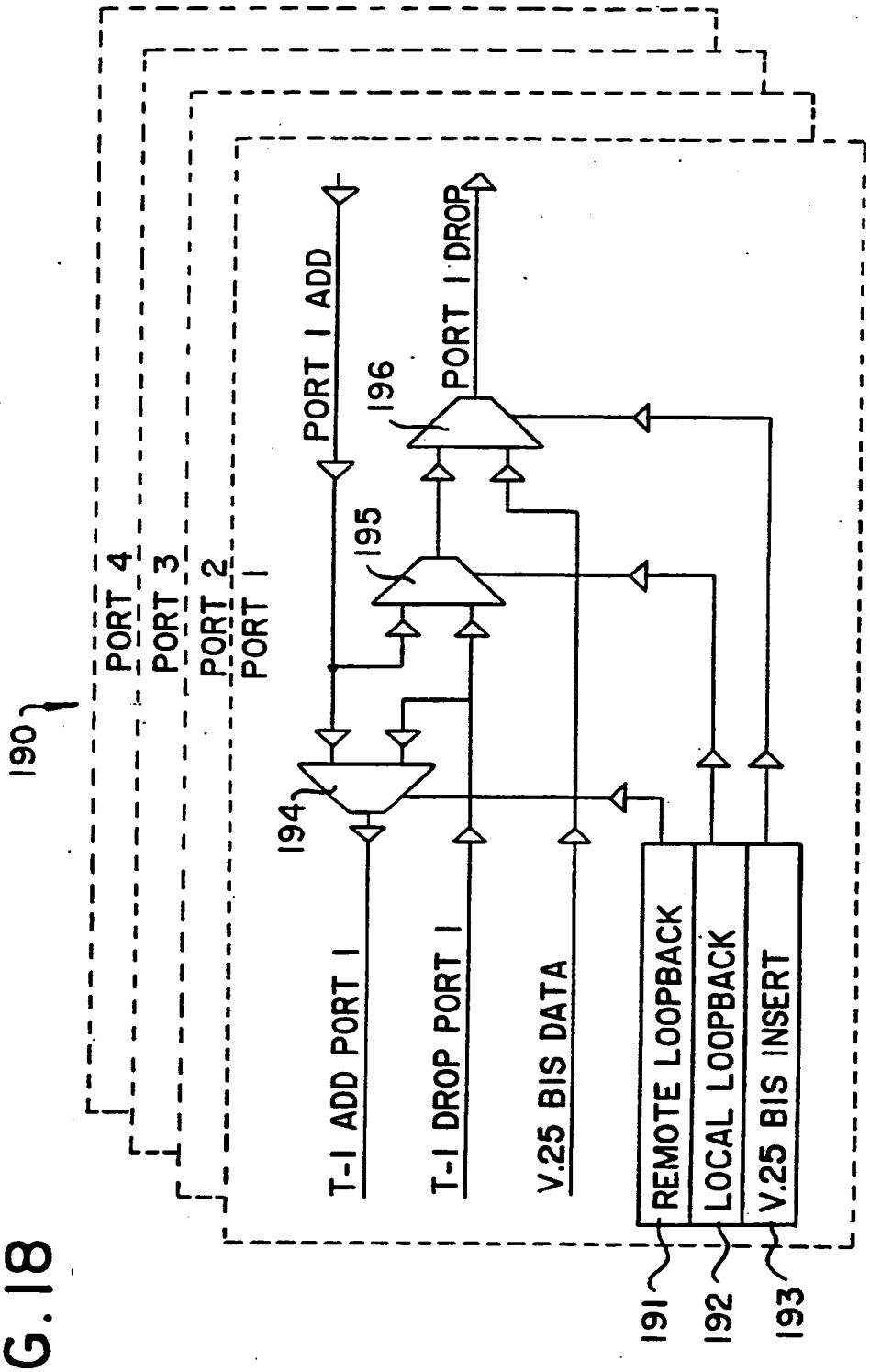


FIG. 18

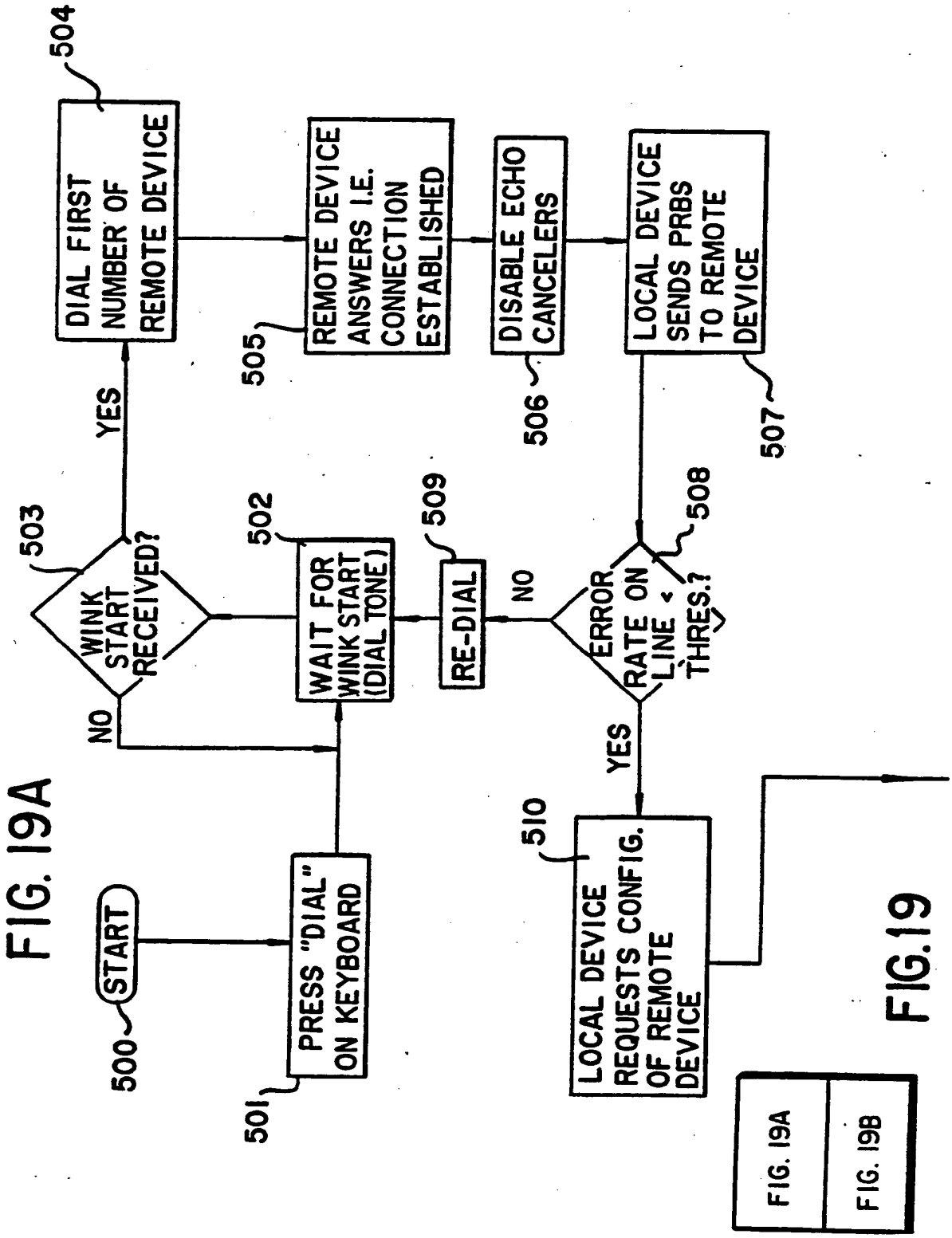


FIG. 19A

FIG. 19

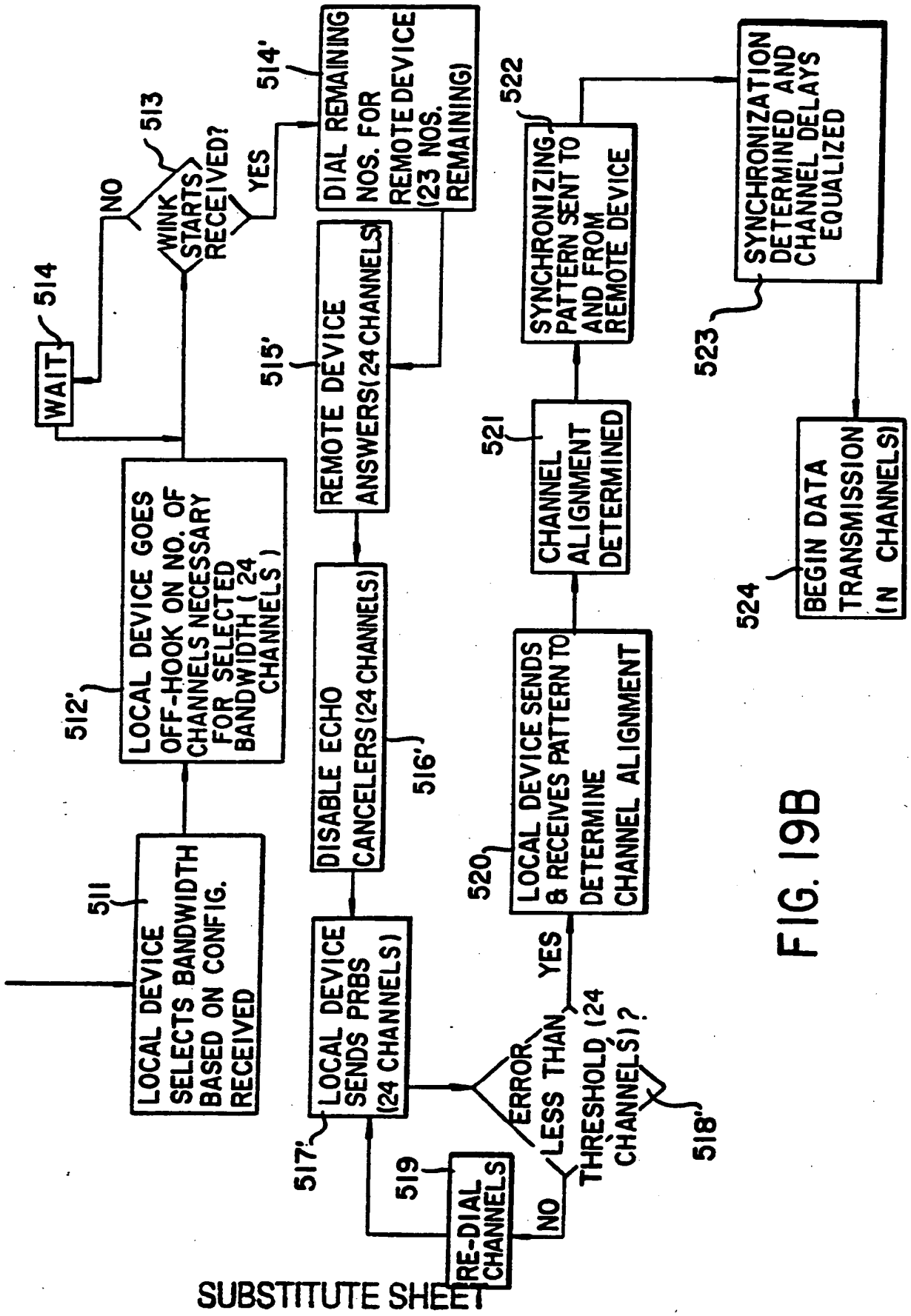


FIG. 19B

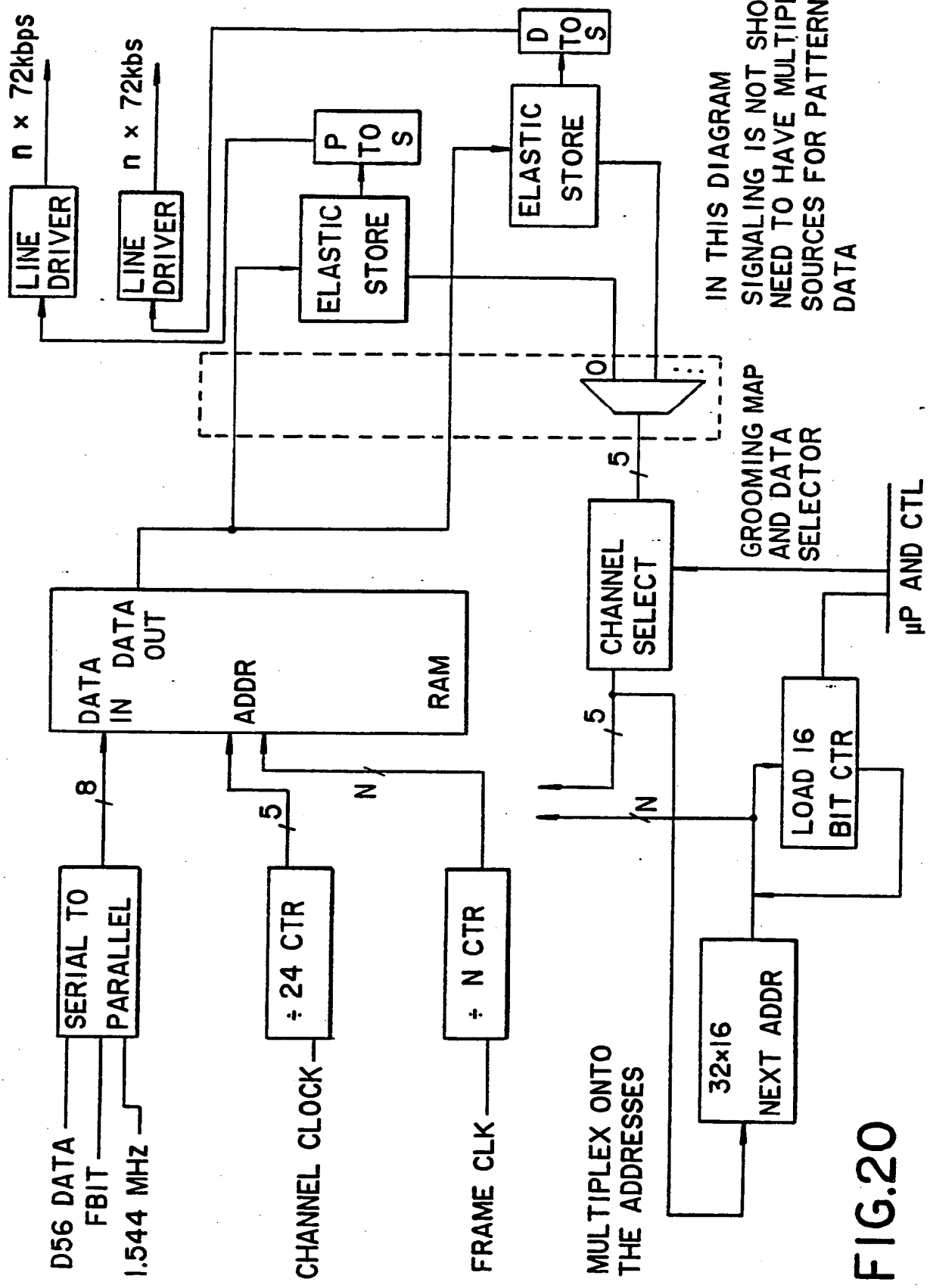


FIG.20

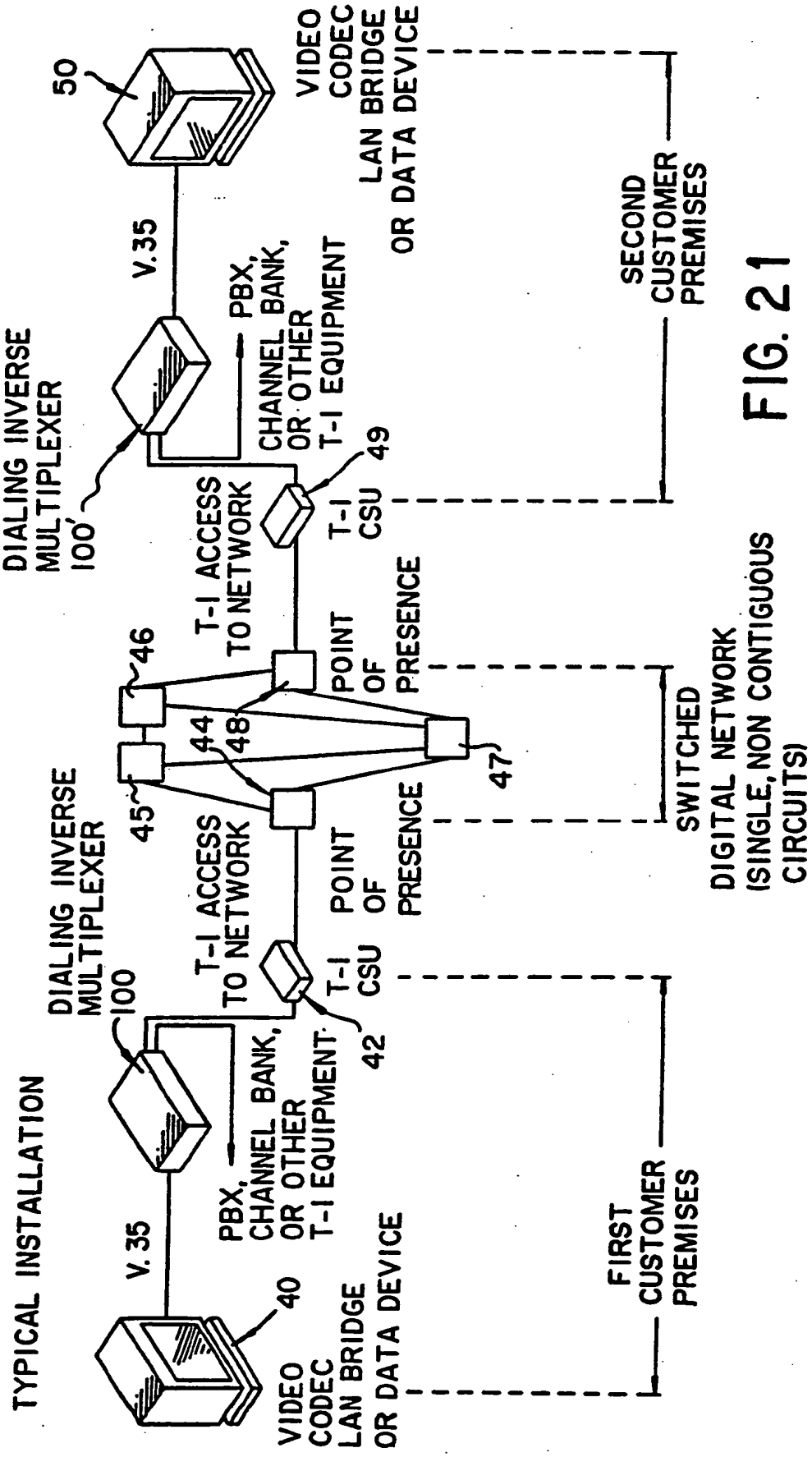
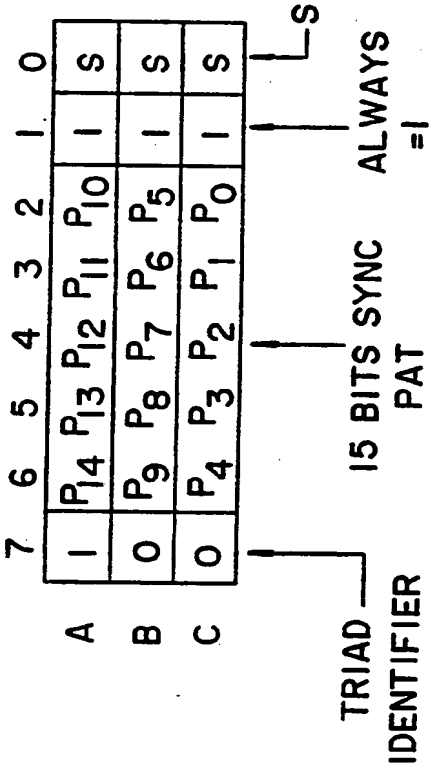


FIG. 21

A= HIGH ORDER PATTERN BYTE
B= MIDDLE PATTERN BYTE
C= LOW ORDER PATTERN BYTE



A 15 BIT PATTERN WILL ACCOMODATE
(2E15) x 125msec DELAY (=2SEC)

FIG.22

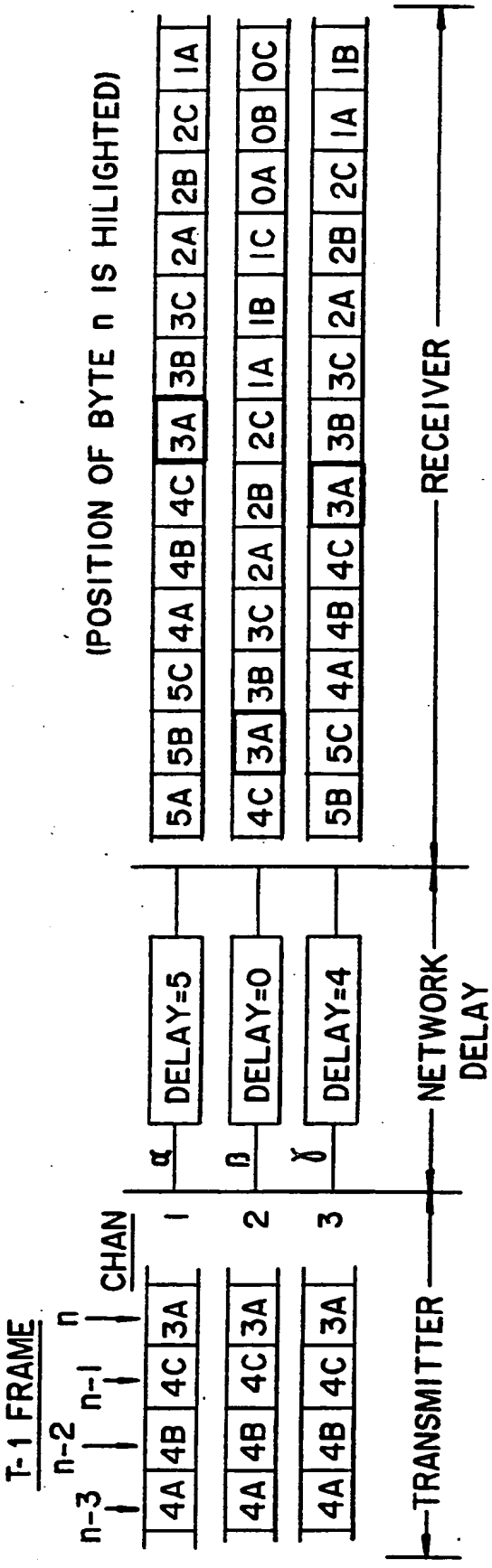


FIG.23

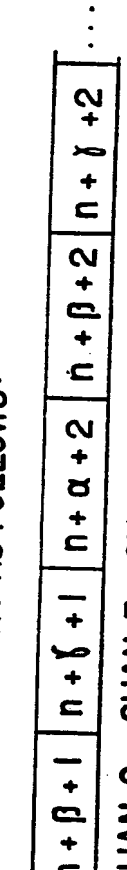


FIG.24

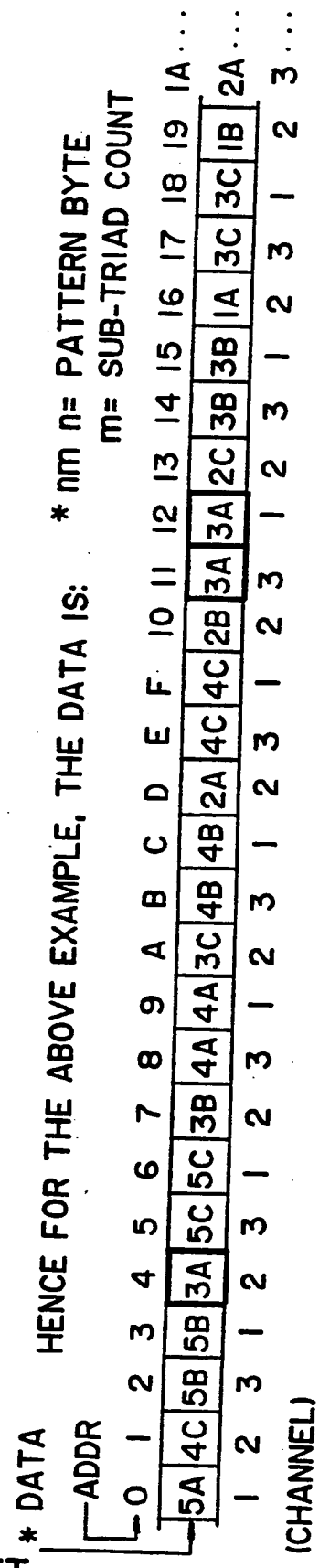


FIG.25

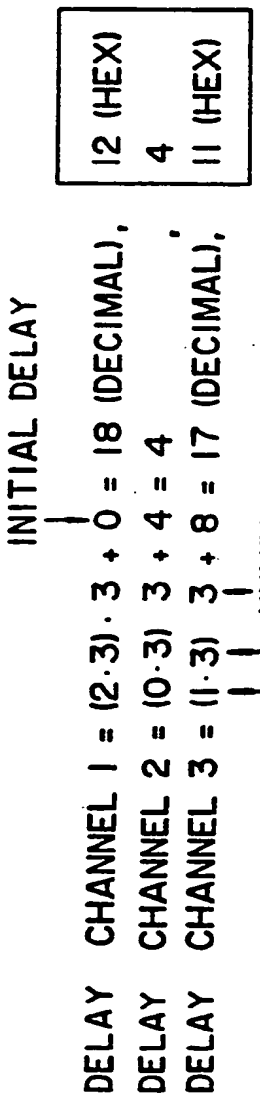


FIG.26

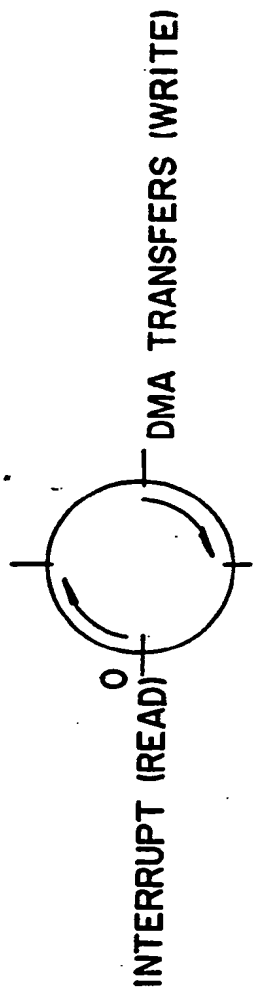


FIG.27

FIG. 28

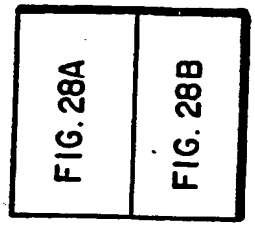


FIG. 28A

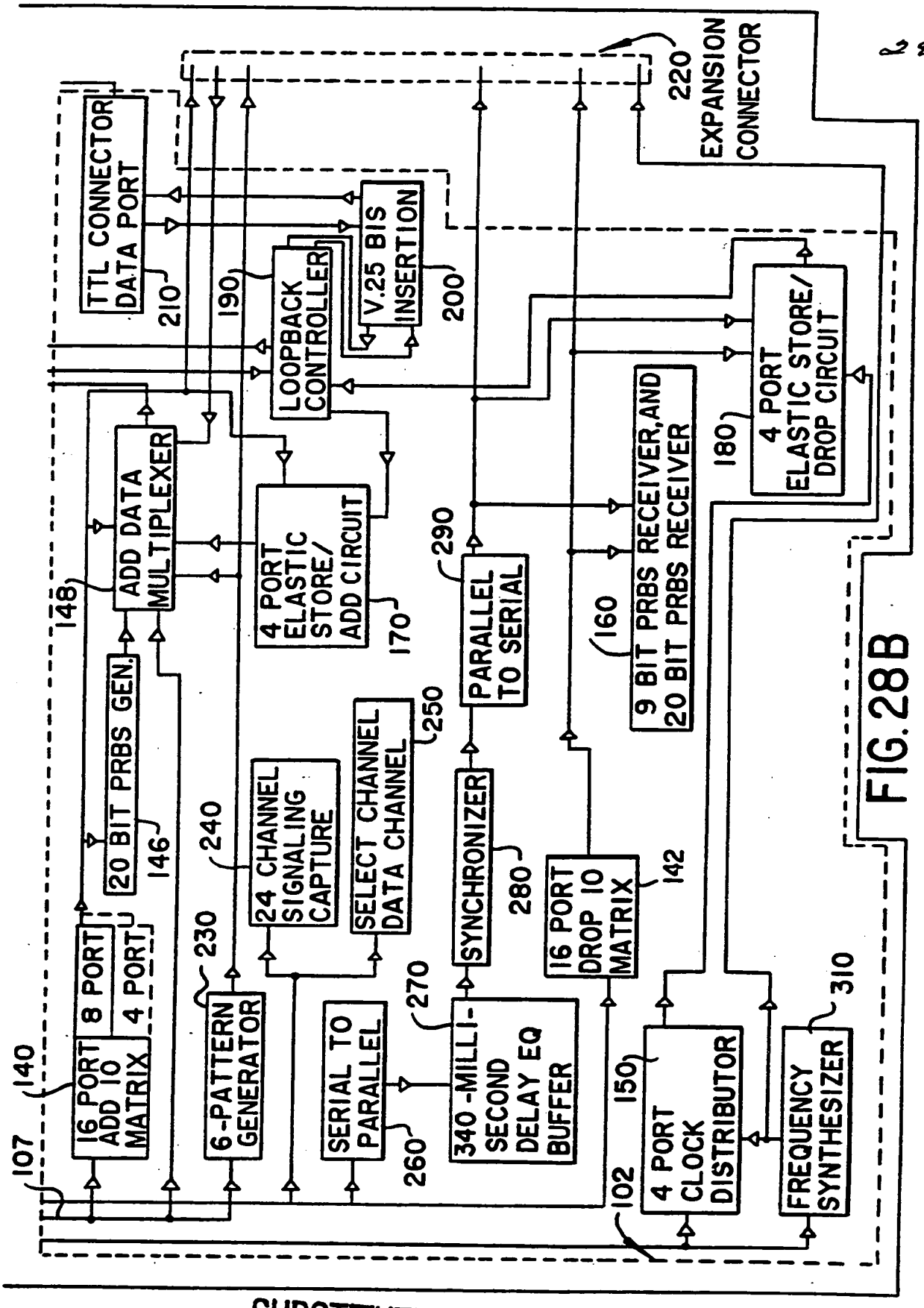


FIG. 28B

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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H04J 3/00

A3

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906,324 30 June 1992 (30.06.92) US

(71) Applicant: DIGITAL ACCESS CORPORATION [US/US]; 11501 Sunset Hills Road, Suite 200, Reston, VA 22090 (US).

(72) Inventor: ROTHRAUFF, Charles, E. ; 11501 Sunset Hills Road, Suite 200, Reston, VA 22090 (US).

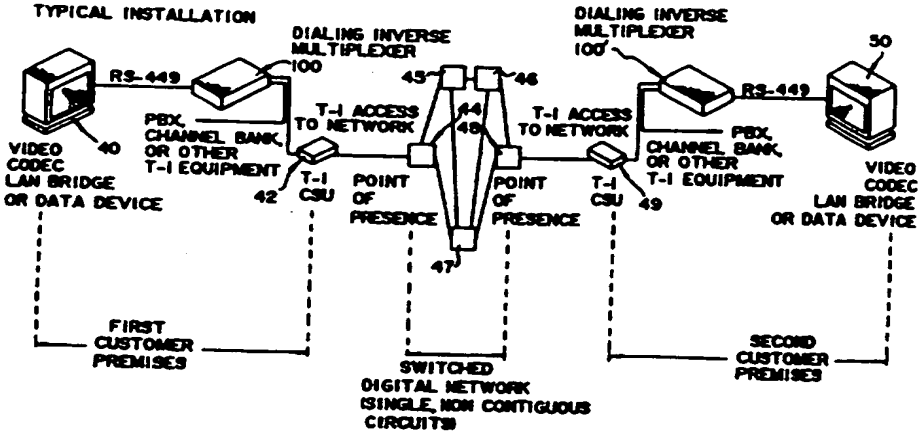
(74) Agents: WESTERMAN, William, F. et al.; Armstrong & Kubovcik, 1725 K. Street, Suite 1000, Washington, DC 20006 (US).

(81) Designated States: AU, BG, BR, CA, CS, FI, HU, JP, KR, NO, PL, RO, RU, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report:
1 April 1993 (01.04.93)

(54) Title: APPARATUS FOR HIGH SPEED DATA TRANSFER



(57) Abstract

The present invention relates to the field of high speed data transfer for digital communications using communications networks having relatively narrow bandwidth time division multiplexed channels. The invention also relates to wideband communications using a plurality of time division multiplex channels having bandwidths which are individually insufficiently large to individually support the wideband communications. The apparatus for data communication includes a first interface arrangement for interfacing with a data communications network; a second interface arrangement for interfacing with a data source; and a data multiplexing arrangement for multiplexing data from the data source into a selected number of channels.

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INTERNATIONAL SEARCH REPORT

International Applic . No PCT/US 92/05888

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl.5 H 04 L 12/00 H 04 Q 11/04 H 04 J 3/00

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl.5	H 04 L H 04 Q H 04 J H 04 M G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	EP,A,0125773 (ABLE COMPUTER) 21 November 1984, see page 4, lines 22-39; abstract; figure 4; claim 1	1,4
Y		2
Y	Derwent's Abstract, no. 83-739 746/33, & SU 965011 (KAPLINSKII N.I.) publ. week 8333	2
Y	Derwent's Abstract, no. 85-29 617/05, & SU 1095442 (BORIN E.A.) publ. week 8505	2
A	US,A,4451827 (STEVEN A. KAHN et al.) 29 May 1984, see abstract	1-2,4

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22-10-1992	25. 02. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	MICHAEL FELHENDLER

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,4825457 (MAYER M. LEBOWITZ) 25 April 1989, see abstract	1-2,4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05888

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. Claims 1,2 and 4
2. Claim 3

See Form PCT/ISA/206 dated 13th November 1992.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1,2 and 4

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9205888 SA 62622

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/01/93
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0125773	21-11-84	US-A- 4547880	15-10-85
		JP-A- 59215154	05-12-84
		CA-A- 1212742	14-10-86
US-A- 4451827	29-05-84	None	
US-A- 4825457	25-04-89	None	

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82